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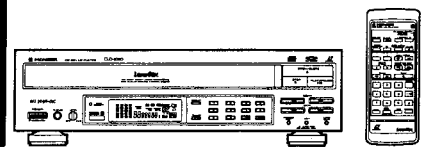
Service Manual



SERVICE GUIDE

ORDER NO.
ARP2063

CD CDV LD PLAYER

CLD-1080

CONTENTS

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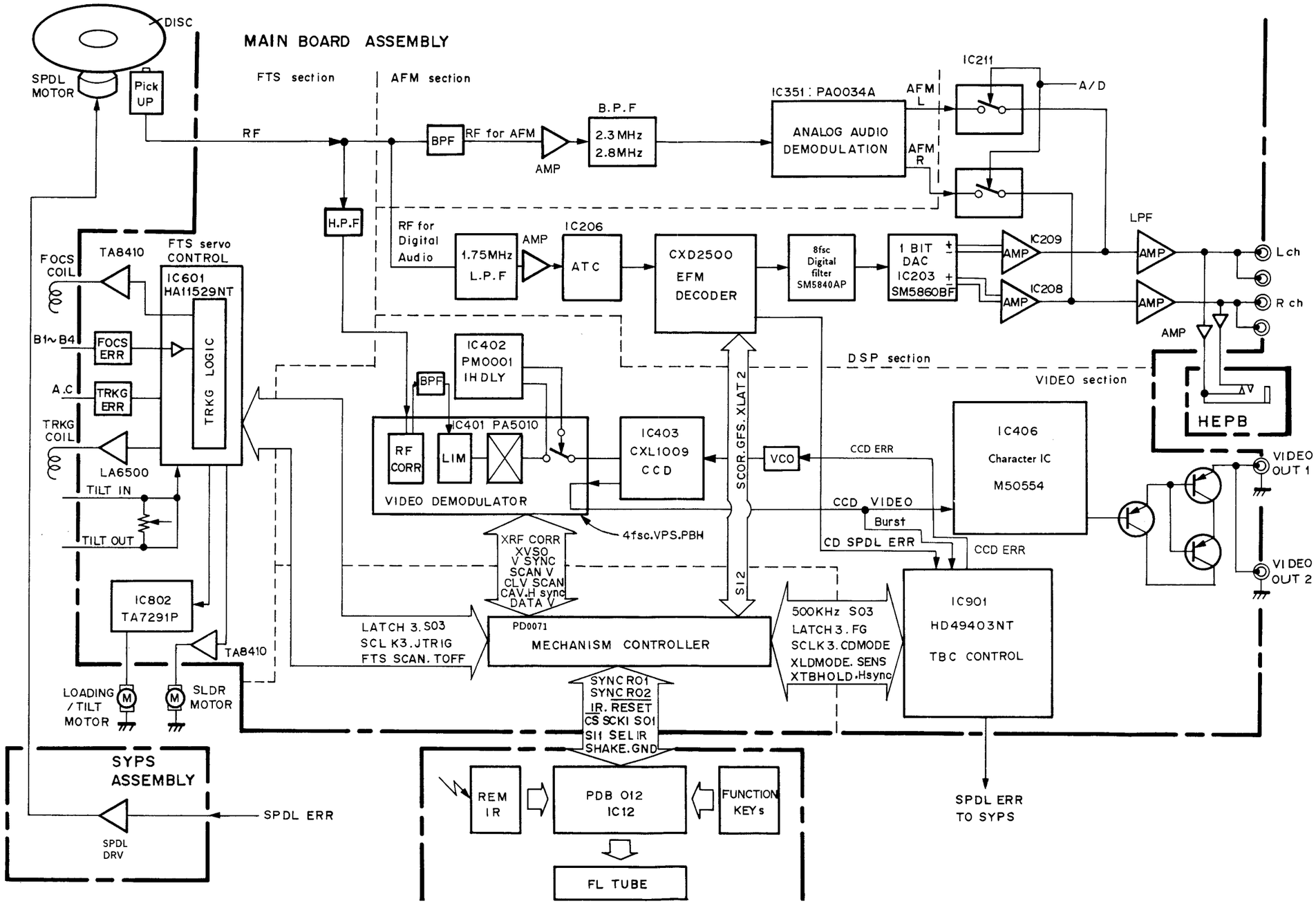
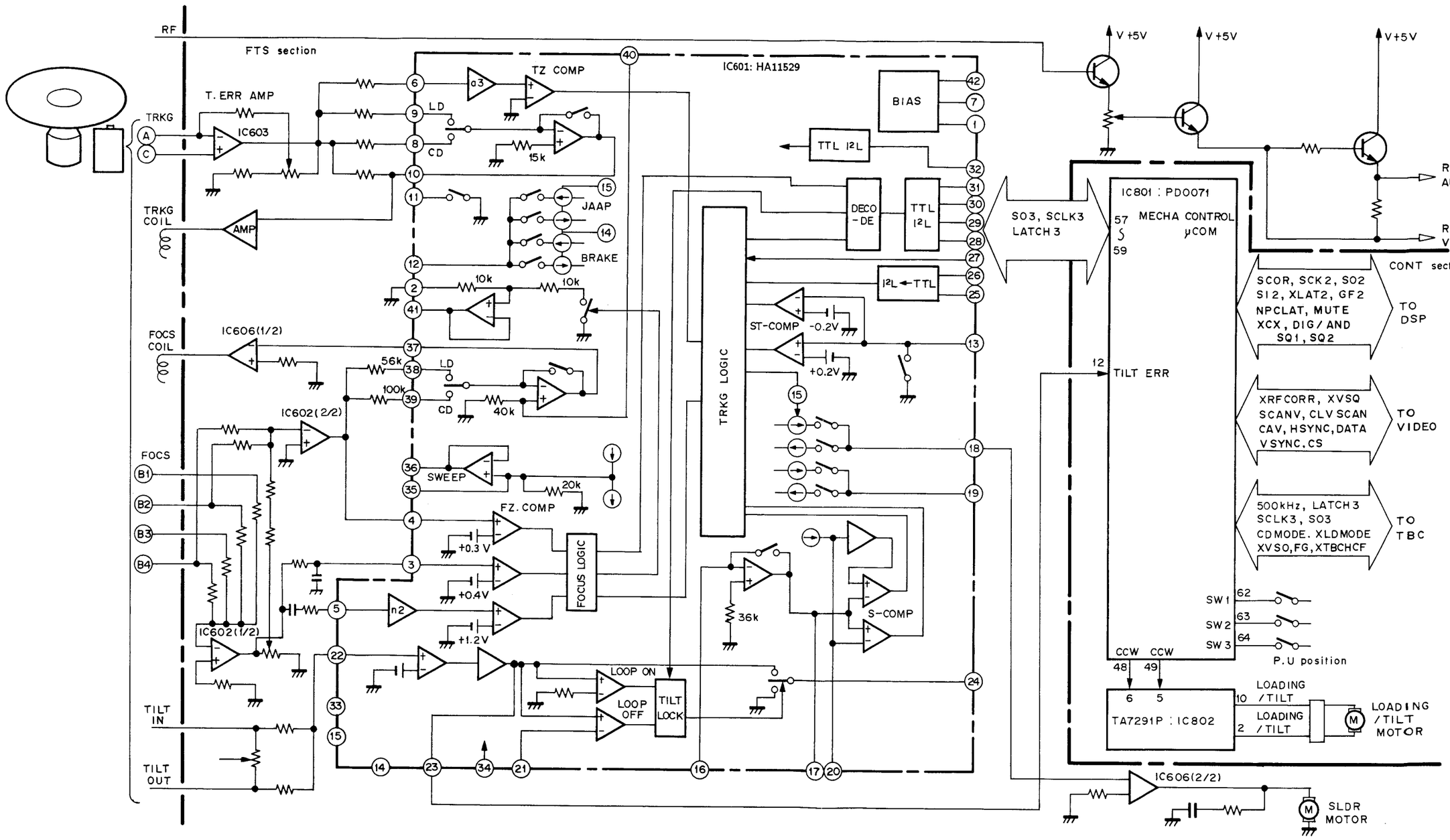
1. OVERALL BLOCK DIAGRAM



FTS BLOCK DIAGRAM (FCS, TRK, SLDR Servo)



2. FOCUS (FCS), TRACKING (TRKG), AND SLIDER (SLDR) SERVOS (Description of HA11529)

(1) Outline

The HA11529 is an analog/digital bipolar IC. It is used by the FTS servos (FOCS, TRKG, and SLDR servos) and has the following functions :

1. FOCS servo control. (It controls the leading-in to the FOCS servo loop. Gain control.)
2. TRKG servo control (loop ON/OFF, track jumping, and brake control during SCAN).
3. SLDR servo control (loop ON/OFF, variable-speed playback, and motor PWM drive).
4. TILT servo control (loop ON/OFF).
5. CD/LD servo characteristic switching. (FOCS, TRKG)
6. The above functions are controlled by the 8-bit serial data which passes through the serial buses (DATA, CLK, LATCH).

The 8-bit serial data's commands are as follows.

MODE	ADDRESS				DATA			
	D7	D6	D5	D4	D3	D2	D1	D0
SCAN MODE CONT	1	0	0	0	SCAN SPEED 1	SCAN SPEED 2	SCAN SPEED 3	1:SCAN ON 0:SCAN OFF
SERVO MODE CONTROL 1	1	0	0	1	FOCS 1:ON 0:OFF	DIRECTION 1:FWD 0:RVS	TILT 1:ON 0:OFF	1: LD 0:CD
SERVO MODE CONTROL 2	1	0	1	0	TRKG Zero cross output 1:1/256 0:Through	TRKG 1:OFF 0:ON	TEST 1:TEST 0:NORMAL	

(2) HA11529 Terminal Functions

Pin No.	Pin Function
1	Vee: −5V
2	FOCS ERROR signal input: OP AMP input to which a SW is connected for gain control during SCAN operation.
3	FOCS SUM input: For DISC detection. Comparator input threshold is + 0.4V.
4	Comparator input threshold for the FOCS S-curve detection is +0.3V.
5	Comparator input threshold for MAIN BEAM ON/OFF track detection is +1.2V. FOCS SUM input.
6	TRKG ERROR input: Comparator input threshold for TRKG ERROR zero cross detection is 0V.
7	GND
8	TRKG ERROR AMP for CD input
9	TRKG ERROR AMP for LD input
10	TRKG ERROR AMP output. TRKG servo phase compensation is connected between this pin and pin 8.
11	Output for switching the TRKG servo loop characteristics during track jump. (Open or Close)
12	Outputs the actuator drive and brake pulse during track jump and the actuator brake pulse during SCAN.
13	Window comparator input to detect the amount of movement in the TRKG actuator during SCAN. Threshold voltage is 0.2V. Actually, an FTS SCAN signal is being input.
14	Current setting terminal for TRKG actuator brake.
15	Current setting terminal for pins other than pin 14.
16	TRKG RTN input : TRKG RTN input for SLDR servo.
17	SLDR servo amp output: During play, the SLDR motor is PWM driven and at that time this pin becomes the window comparator input.
18	SLDR drive signal output during play or when high speed slider is in operation.
19	SLDR drive signal output when SLDR in operating at low or mid speeds. (Not used.)
20	Capacitor connected pin for setting the slope of the reference triangular wave for the SLDR motor PWM drive during play.
21	Resistor connected to set comparator threshold for turning off the TILT servo drive.
22	TILT ERROR input: OP amp input.
23	A VR is connected for setting the TILT servo gain with the output of the OP amp from pin 22.
24	Output for TILT motor drive.
25	T-CROSS output : TRKG ERROR zero cross count output. Depending on the serial data command, output may be divided by 256.
26	F-LOCK output: "Low" when FOCS lock activated.
27	J-TRIG input: Triggered at startup. "Low" under normal operating conditions.
28	RESET input:
29	LATCH input: Serial interface bus to the system CPU.(pins 29,30,31) Data is latched on the trailing edge.
30	SDATA input: 8-bit serial command data input.
31	SCLK input: clock for serial data transmission.
32	500kHz input: internal logic clock input. About 450kHz.
33	TEST pin: Normal state is "Low". (Not used.)
34	Pin for setting the injection current used by internal I^2L logic.
35	Capacitor connected pin for setting the lens UP/DOWN cycle when FOCS ON is activated.
36	Drive voltage output for lens UP/DOWN.
37	FOCS ERROR amp output: FOCS servo phase compensation is connected between pins 38 and 39.
38	FOCS ERROR amp LD input.
39	FOCS ERROR amp CD input.
40	Pin with connected offset adjustment VR that uses the uninverted FOCS Error amp input.
41	Op amp output for FOCS gain control. (Not used.)
42	Vcc: +5V.

(3) Function Description

FOCS System

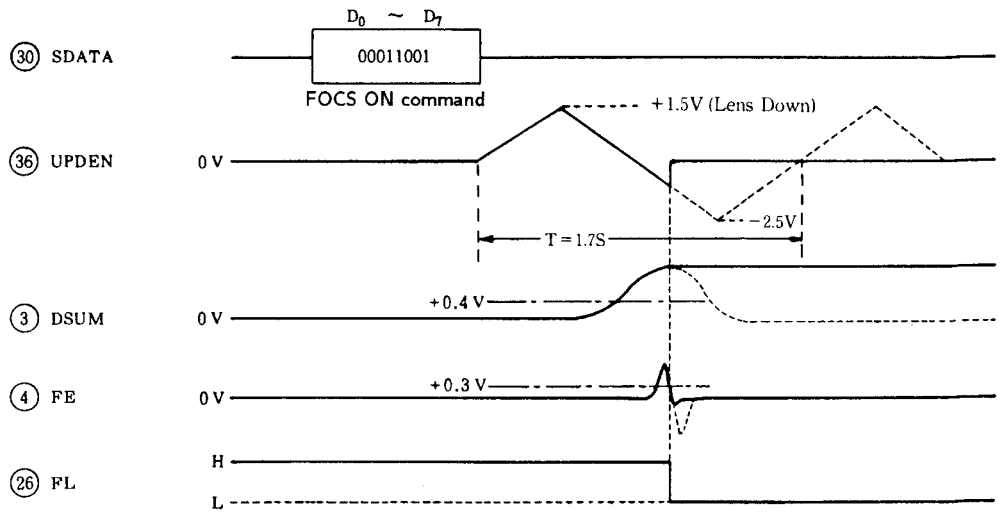
1. FOCS leading-in operation

The FOCS servo leading-in operation is executed when the objective lens is moved UP or DOWN and the DSUM (pin 3) and the FE (pin 4) inputs turn ON the FOCS loop when the FOCS lock conditions are met.

If defocusing occurs due to disc scratches, etc., a voltage of +0.6 V will be output to output pin 36 for about 0.5S when the FOCS servo loop is turned OFF. The lens will then switch to the UP operation again.

2. FOCS down and leading-in again

During playback, if the DSUM (pin 3) input falls to +0.4 V or less due to disc scratches, external vibration, etc., the abnormal condition will be detected and the FOCS servo loop will turn OFF. At the same time, the objective lens will go UP or DOWN automatically and turn ON the FOCS servo loop when the conditions described in "1." are met.



* The dotted line indicates the waveform when the FOCS servo loop is not ON.

Fig. FOCS servo pull in Timing Chart

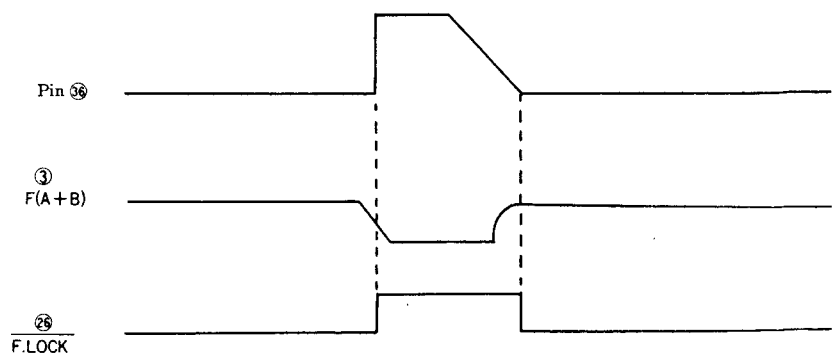
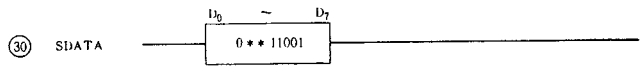


Fig. Defocus Timing Chart

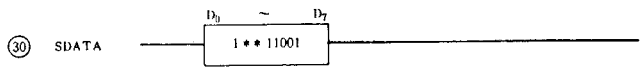
3. CD/LD switching

The FOCS servo's loop gain and phase compensation characteristics are switched depending on the type of disc (CD or LD) being played back. The serial data bit for switching between CD and LD is in the same address as the FOCS ON command bit. Both can be set with a single transfer.

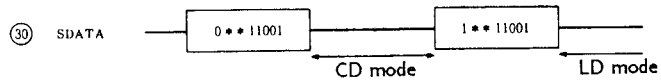
i) Focus ON command when the CD mode is set.



ii) FOCS ON command when the LD mode is set.



iii) When the CD/LD mode is switched during playback (CD mode → LD mode).



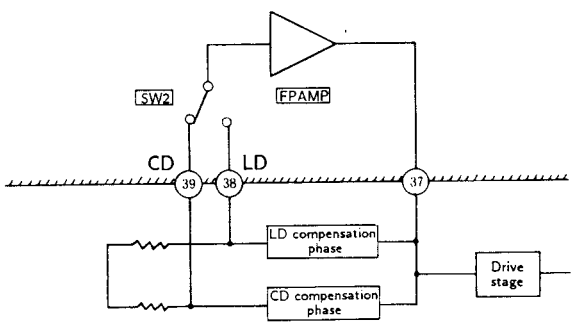


Fig. CD/LD switching

TRKG System

1. Track jump operation

The track jump starts when the jump trigger input's startup edge is received from JUMP (pin 27). The acceleration/deceleration pulse is switched by looking at the tracking error's zero cross. Also, SW12 and SW24 will operate in concert during the jump period. SW12 is used for switching the TRKG loop characteristic and SW24 is used for the TRKG error's zero cross phase adjustment.

The forward jump or reverse jump is switched by the serial data transfer.

The jump trigger signal controls the input signal to 6P so that it becomes advanced in phase.

i) Forward Jump

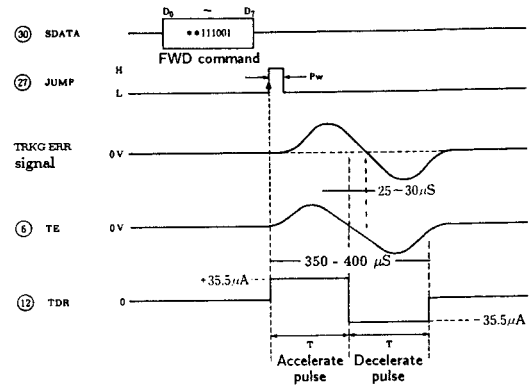
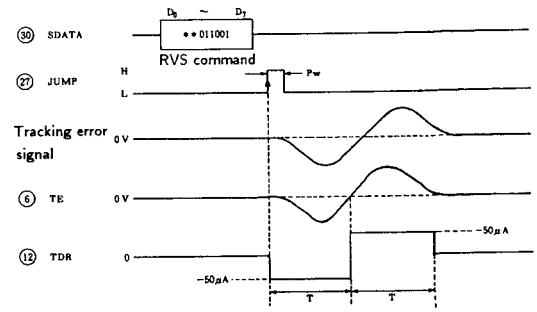


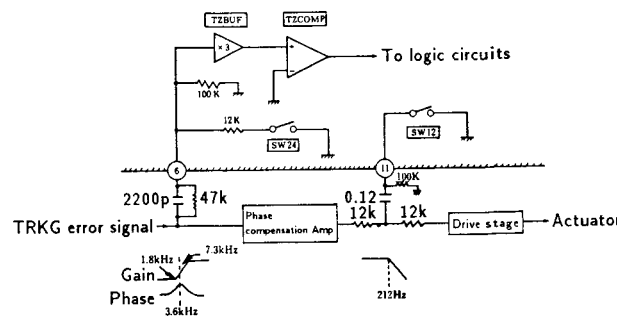
Fig. FWD JUMP Timing Chart

ii) Reverse Jump



Note: The jump trigger signal is normally LOW. The pulse width of Pw is set at 30μS.

Fig. Reverse jump Timing Chart



2. Scan operation

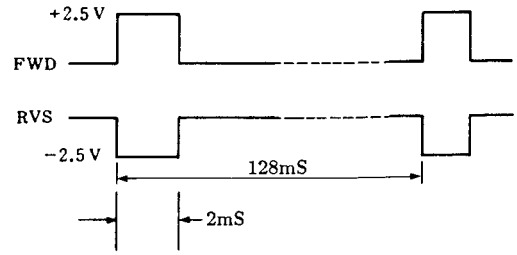
During low- to medium-speed scanning, the TKRG servo detects the actuator's displacement with the ST (pin 13) input. Then it turns OFF the loop and turns it ON again when TE's (pin 6) error signal falls below the stipulated frequency.

During the loop OFF period, the brake pulse will be output from TDR (pin 12) based on the timing chart below. The polarity of the timing pulse will be determined by the polarity of the signal that is input to ST (pin 13), rather than by the serial data transfer's direction setting. The brake pulse's duty is automatically set to five steps (50% - 100%) according to the actuator speed detected by TE (pin 6). Also, the adjustment of the brake current IB is enabled by BEST (pin 14).

In order for the system controller to determine the TRKG servo loop's open and closing timing during SCAN for 13P, the FTS SCAN signal below is input.

This signal is input to pin 12. Since its polarity is reverse that of the brake pulse, it improves the convergence during braking.

The FTS SCAN signal's cycle will be 128 mS.



i) Forward scan

T.OFF changes FOCS BAL signal to optimize TRKG open/close during SCAN mode.

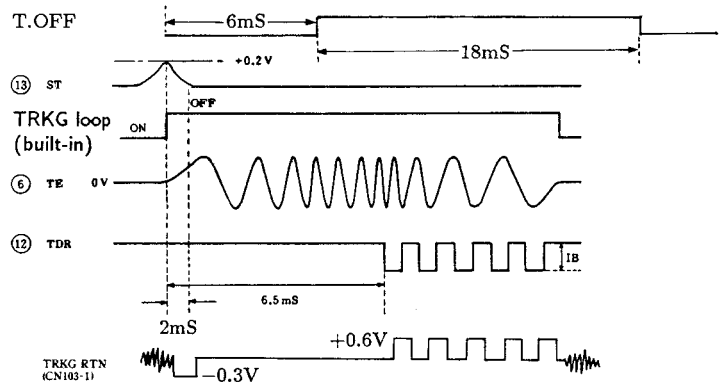


Fig. Forward Scan Timing Chart

ii) Reverse scan

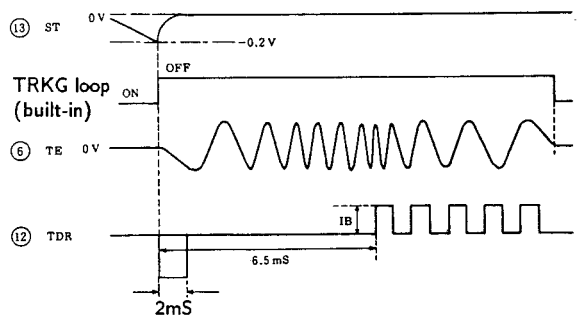
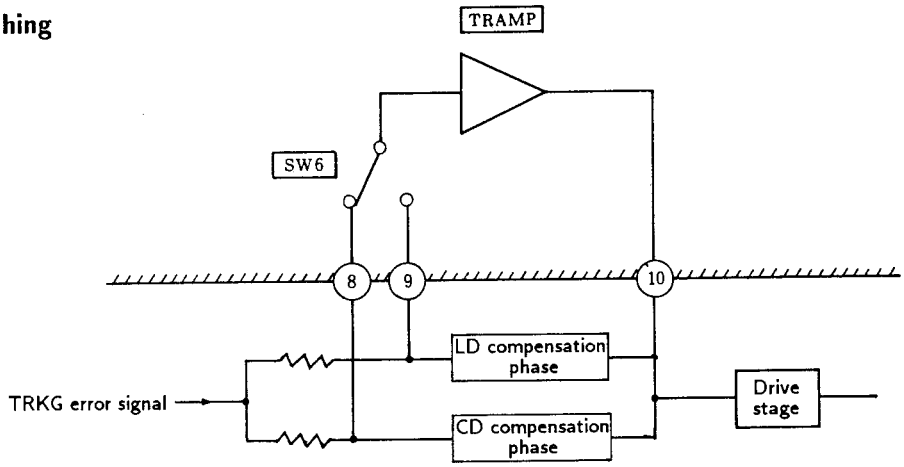


Fig. Reverse Scan Timing Chart

3. CD/LD switching

CD/LD switching can be done in the same way as for FOCS servo CD/LD switching.

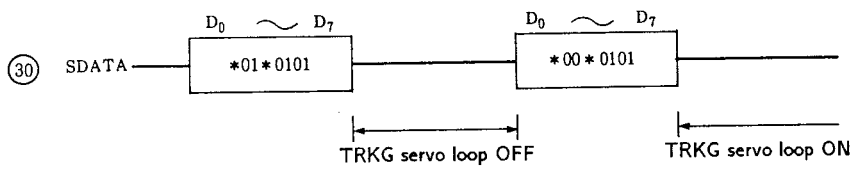
CD/LD switching



4. TRKG loop ON/OFF control

The TRKG loop can be switched ON or OFF by the serial data transfer.

TRKG servo loop ON/OFF



5. TRKG count

The track passing count during high-speed scanning which are counted by the FTS control IC are through output from TCNT(pin 25).

This signal is used for the misclamp detection when playback starts and the track count during CD search.

After playback starts, the misclamp detection sets the TRKG servo to an open loop. If there are 1,600 track passes (TRKG count, 5 passes : Approx. 1mm eccentricity) for one disc revolution (for FG24), it will be deemed normal. Any more track passes will be deemed as a misclamp and the disc will be ejected.

Slider System

1. Normal playback mode operation

During normal playback, the TRKG actuator drive current's DC component undergoes PWM modulation by SCOMP1 and SCOMP2. This PWM pulse turns ON SW16 and SW17 and outputs the drive signal.

The inclination of the standard triangular wave can be changed by the capacitor connected to SLP (pin 20).

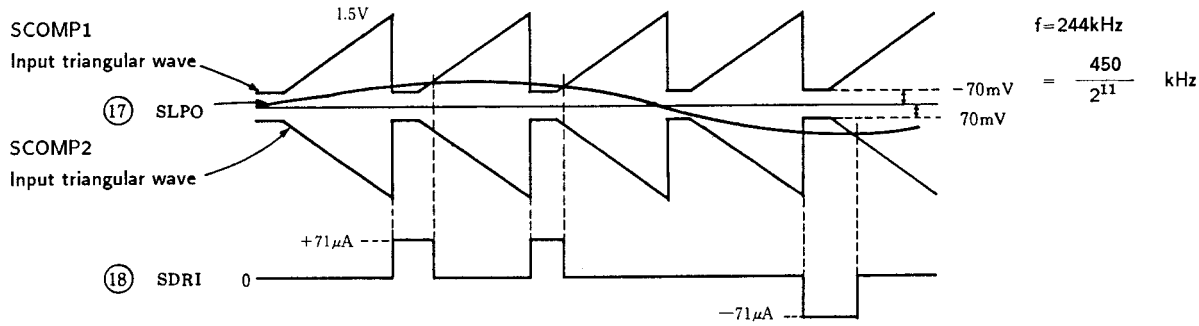


Fig. SLDR servo Operation

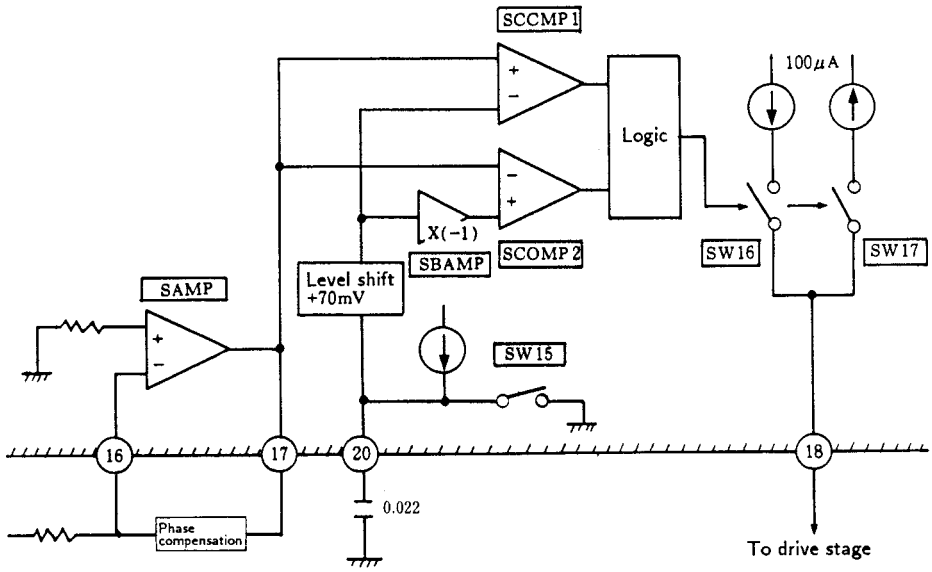


Fig. Serial Data transfer during Scan mode Operation

2. Scan mode operation

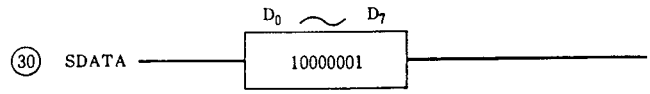
During a scan operation, the SLDR servo loop is turned OFF and the signal for the speed set by the serial data transfer is output from SDR1 (pin 18).

i) High-speed scanning

With the serial data transfer shown on the right, SW16 or SW17 can be turned ON. A $\pm 100\mu$A drive signal is output from SDR1 (pin 18).

The direction will go according to the serial data transfer's direction setting.

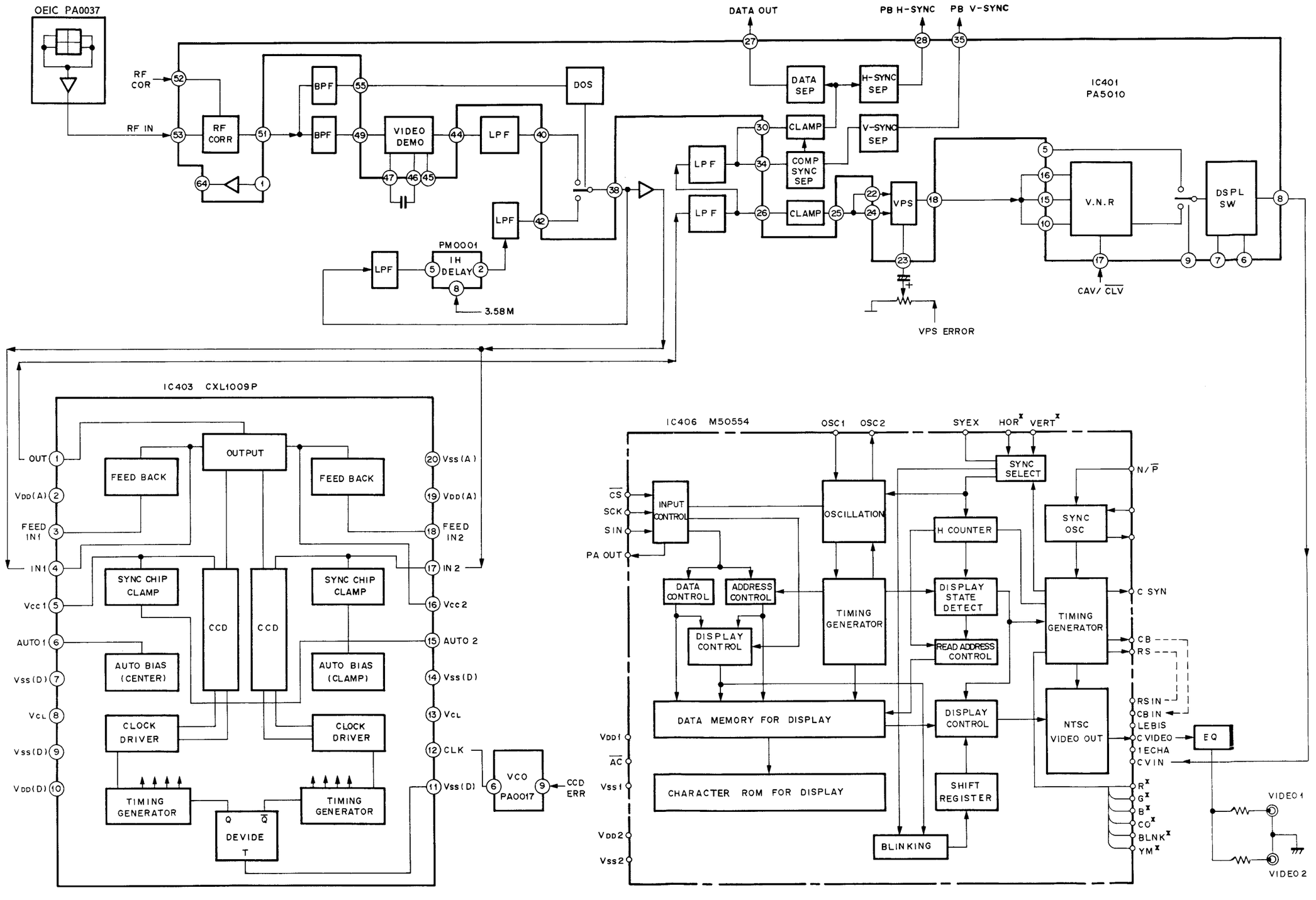
With the pairing of the 10000001 high-speed scan command and the 10001110 SLDR servo loop OFF command, the SLDR's drive voltage is controlled and the scan speed is set.



ii) Low- to medium-speed scanning

The player doesn't use HA11529 pin 19, so the scan speed is set by duty ratio. The same as the high-speed scanning described above.

VIDEO SIGNAL BLOCK DIAGRAM



3 VIDEO SIGNAL DESCRIPTION

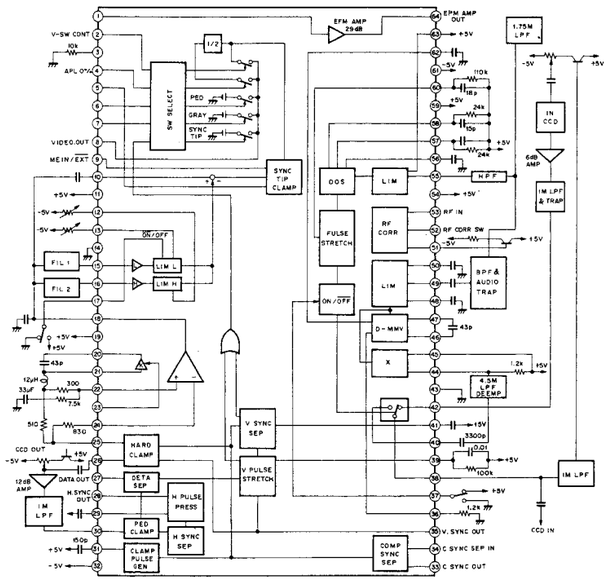
3. 1 PA5010 Description

After the RF signal (output from PA0037 on the pickup Ass'y) undergoes gain adjustment, it is input to pin 53 of PA5010. The signal undergoes RF correction. Then its waveform is shaped by the internal limiter circuit and the signal is demodulated. The demodulated video signal passes through the 5MHz low-pass filter and the de-emphasis circuit. Then it is re-input from pin 40. At the same time, it undergoes dropout detection by DOS (dropout sense). If there is any dropout, the internal SW is switched so that the 1H delayed video signal is inserted.

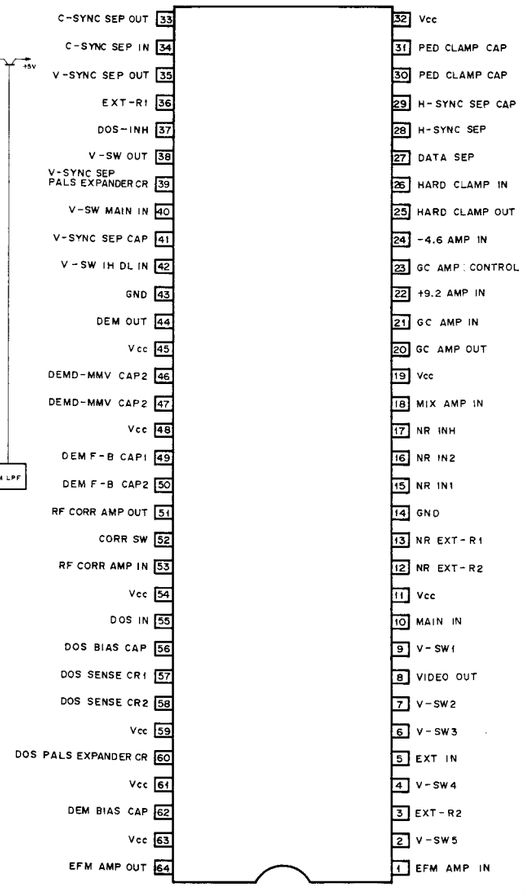
The video signal that is output from pin 38 of PA5010 is input to pins 4 and 17 of IC403 CXL1009. This is where the time base error's high-frequency component generated by the disc's eccentricity, etc., is removed.

The CCD video signal that is output from pin 1 of IC403 is input to pin 26 of IC401. The pedestal section is key clamped. Then after passing through the VPS (Video Phase Shifter) and VNR (Video Noise Reduction), the signal is output from pin 8. Also, the composite sync (PB-C sync), playback vertical synchronizing signal (PB-V Sync), playback horizontal synchronizing signal (PB-H Sync), and the V blanking period data (Philips code) are extracted from the video signal that is input from pin 34.

PA5010 Internal Block Diagram



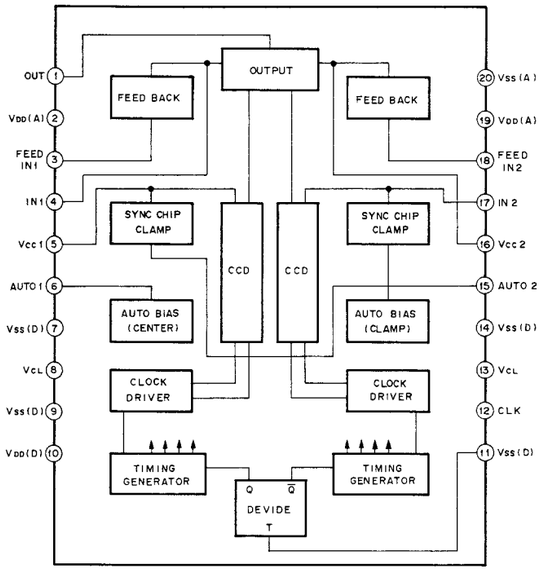
PA5010 External View



3. 2 CXL1009 Description

PA5010 output pin 38's video signal is input to pins 4 and 17 of CXL1009. CXL1009 is a CMOS CCD-dedicated IC. The clock time is controlled by the error signal obtained by the phase comparison between the burst signal and the reference signal (3.58MHz). The CCD variable delay line's delay time is thereby changed.

CXL1009 Internal Block Diagram



CXL1009 Pin Description

PIN No.	SYMBOL	I/O	PIN DESCRIPTION
1	OUT	O	OUTPUT
2	VDD (A)		Power supply input 1 (analog)
3	FEED IN1	I	Feedback input 1
4	IN1	I	Input 1
5	VCC1	I	Gate 1
6	AUTO1	O	Auto Bias 1
7	Vss(D)		GND (digital)
8	VCL		Power supply input 2(digital)
9	Vss(D)		GND (digital)
10	VDD(D)		Power supply input 1(digital)
12	CLK	I	Clock input
13	VCL		Power supply input 2(digital)
14	Vss(D)		GND(digital)
15	AUTO2	O	Auto Bias 2
16	VCC2	I	Gate 2
17	IN2	I	Input 2
18	FEED IN2	I	Feedback input 2
19	VDD(A)		Power supply input 1(analog)
20	Vss(A)		GND(analog)

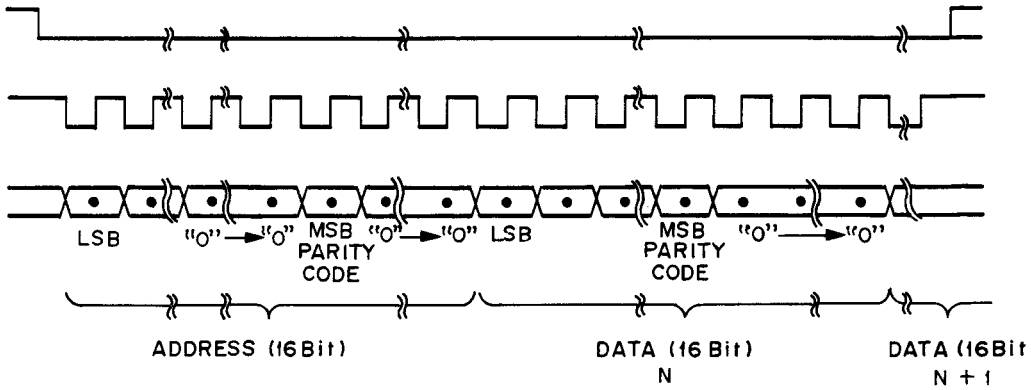
3. 3 M50554 Description

M50554 is an IC which uses the silicon gate CMOS process and controls the TV screen character and pattern displays. The video signal demodulated by PA5010 is input to pin 13 (CVIN) of M50554. During superimposition, it overlays the character output.

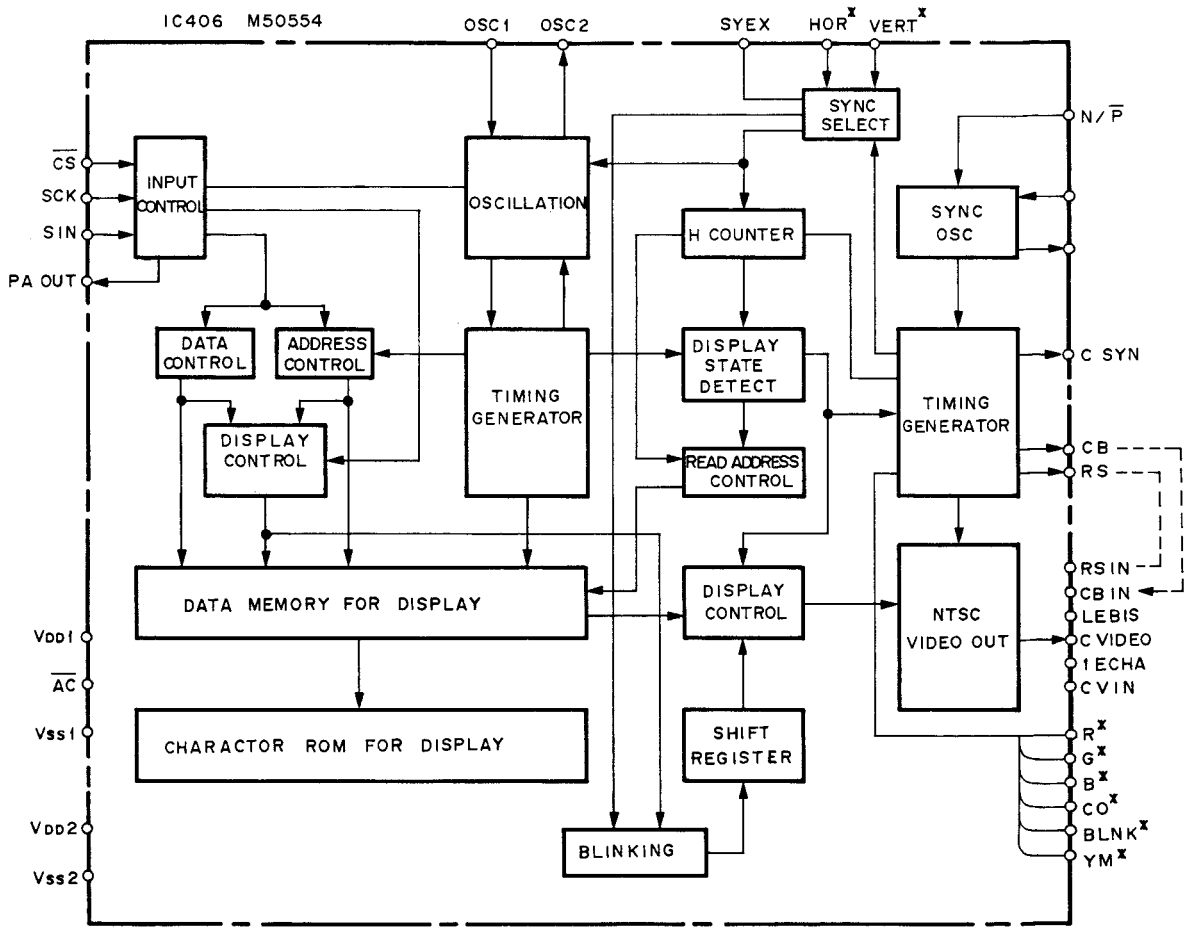
The character data consists of 16 bits. The lower 11 bits contain the data, the next bit contains the parity code, and the data of the remaining upper 4 bits are all 0. The character data is input from pin 8 (SIN) in serial.

The address consists of 16 bits. The lower 8 bits are the effective address. The next 3 bits are 0. The next bit is the parity code and the data of the remaining upper 4 bits is all 0. After CS signal shutdown, SCK's 16 bits become the address. For the input data thereafter, the address is incremented for every 16 bits.

M50554 Data Configuration



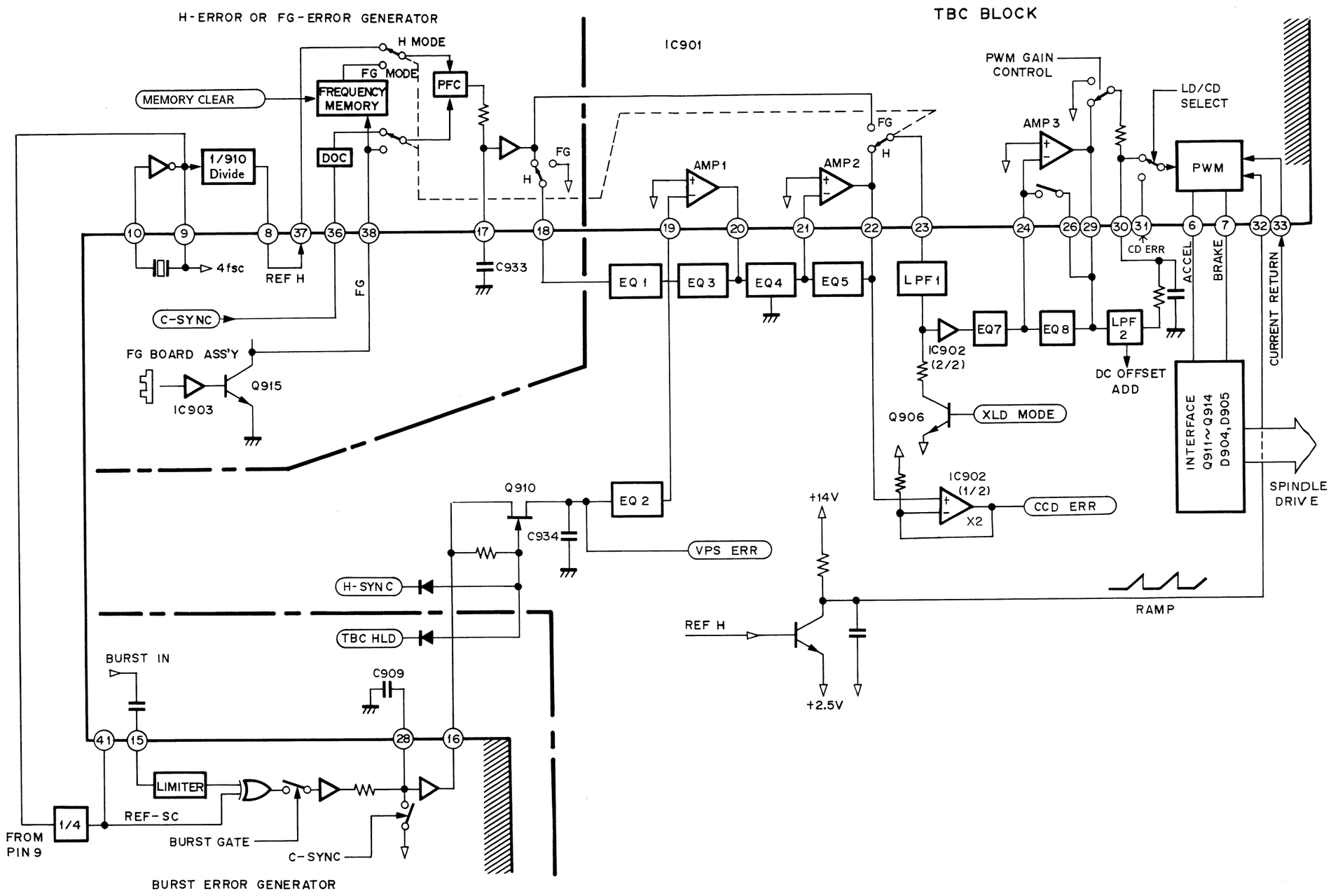
M50554 Internal Block Diagram



M50554 Pin Description

No.	SYMBOL	PIN NAME	DESCRIPTION
1	Vss1	Ground terminal	Connect to GND with the digital circuit's ground terminal.
2	SCK	Serial clock input	When the CS terminal is "Low", the SIN serial data will be taken when SCK starts up. Hysteresis input. Pull-up resistor is built-in.
3	AC	Auto clear input	When "Low" , the IC's internal circuit is reset. Pull-up resistor is built-in. Hysteresis input.
4 5	OSC1 OSC2	External oscillation circuit	These terminals are for an externally-attached oscillation circuit for the display. The standard oscillation frequency is about 7 MHz. This oscillation frequency determines the TV screen horizontal direction's display position and the character width.
6	N/P	NTSC/PAL switching input	This is a synchronizing signal generation switching terminal for NTSC or PAL. When "H", the NTSC synchronizing signal will be generated. And when it is "L", the PAL synchronizing signal will be generated. Pull-up resistor is built-in.
7	CS	Chip select input	This is the chip select terminal. It will be set to "L" for serial data transfers. Pull-up resistor is built-in.
8	SIN	Serial data input	The data and address of the display control register and the display data memory are input as serial. Pull-up resistor is built-in.
9	PAOUT	Parity output	This is an odd parity output which does 1 bit error detection on the SIN's 1 word.
10	SYEX	Synchronizing signal switching input	This is a switching terminal for the external synchronizing signal or the internal synchronizing signal. When "H," it will be set to the external synchronizing signal mode. And when "L," it will be set to the internal synchronizing signal mode. The SYEX consists of EX registers for addresses 2, 4, and 3 in the display control register, and the internal synchronizing priority's logical sum. Pull-up resistor is built-in.
11	Vss2	Ground terminal	Connect to GND with the analog circuit's ground terminal.
12	CVIDEO	Composite video output	This is the composite video signal's output terminal. It outputs a 2Vp-p composite video signal. During a superimposition, the signal is output after the character output, etc., is layered on the CVIN signal.
13	CVIN	Composite video input	This is the composite video signal's input terminal. During a superimposition, the character output, etc., is layered on the composite video signal.
14	LEBK	Blanking level	This is an input terminal which determines the video signal's blanking level.
15	LECHA	Character level input	This is an input terminal which determines the character output level in the video signal. The color of the characters will be white.
16	CBIN	Color burst signal input	The CB output is converted into the video signal's color burst signal level by the external circuit and then input.
17	RSIN	Character background carrier chrominance signal input	The RS output is converted into the video signal's carrier chrominance signal level by the external circuit and then input.
18	VDD2	Power terminal	Connect the analog circuit's power terminal to a +5 V power source.
19	RS	Character background carrier chrominance signal output	This is a carrier chrominance signal output for coloring the character background. It outputs a signal which has a phase angle with respect to the color burst signal CB. Amplitude is 5 V.
20	CB	Color burst signal output	A 3.58 kHz color burst signal is output for NTSC, and a 4.43 kHz color burst signal is output for PAL. Amplitude is 5 V.
21	YM	Luminance signal output	This is the luminance signal output. When the font ROM is determined, the polarity can be selected.
22	BLNK	Character background output	The character background signal is output. When the font ROM is determined, the polarity can be selected.
23	CO	Character output	The character signal is output. When the font ROM is determined, the polarity can be selected.
24	B	Blue output	This is the blue output terminal. When the font ROM is determined, the polarity can be selected.
25	G	Green output	This is the green output terminal. When the font ROM is determined, the polarity can be selected.
26	R	Red output	This is the red output terminal. When the font ROM is determined, the polarity can be selected.
27	CSYN	Composite synchronizing signal output	The NTSC or PAL composite synchronizing signal is output. The polarity is negative and the amplitude is 5 V.
28 29	OSCOUT OSCIN	Synchronizing signal generation oscillation	These terminals are for the external synchronizing signal generation oscillation circuit. It uses a 14.32 MHz oscillation frequency for NTSC and a 17.73 MHz oscillation frequency for PAL.
30	HOR	Horizontal synchronizing signal	The horizontal synchronizing signal is input. Hysteresis input. When the font ROM is determined, the polarity can be selected.
31	VERT	Vertical synchronizing signal	The vertical synchronizing signal is input. Hysteresis input. When the font ROM is determined, the polarity can be selected.
32	VDD1	Power supply input	Connect the digital circuit's power terminal to a +5 V power source.

TBC(Time Base Corrector) BLOCK DIAGRAM



4 TBC SECTION OUTLINE

The player's time base corrector corrects the playback signal's comparative low-frequency error component with the spindle servo. Also, it corrects the high-frequency component (due to the disc's eccentricity) with the CCD servo, and it corrects the residual jitter component with the CPC error detection circuit.

4. 1 Spindle Servo

The player's spindle servo uses the PFC (same as TC5081) to produce the H error. Compared to the trapezoid, the PFC phase detection precision is low. Therefore, the loop mainly consists of the burst error. The loop is thus comprised of the addition of the burst error and the H error.

Multiple phase lock points are created where the direct current output of both phase comparators is balanced. The error signal that goes to the CCD passes through IC901 (1/2) and makes the direct current before the IC901(1/2) as the spindle servo's error. As a result, when the CCD loop is opened at the compulsory point, the spindle servo's gain setting is thrown off, disabling the locking of the spindle servo.

4. 2 Spindle Motor Runaway Detection System

The player's runaway detection system is very different from that of previous models. The player's runaway detection system relies largely on the FG (frequency generator) signal obtained by the FG sensor which is attached to the spindle motor. When the spindle motor starts up, it accelerates to about 1600 rpm. It then reaches 1800 rpm by the FG servo and enters the H loop. For CAV discs, if the spindle motor is unlocked, it will reach 1800 rpm by the FG servo and enter the H loop.

For a CLV disc, the rpm's FG frequency when the spindle motor is locked is stored in memory. When the lock is released, the rpm before the unlocking by the FG servo is taken from memory and input to the H servo.

4. 3 Spindle Motor Gain Control

The spindle motor's gain control is also different from that of previous player models. It is dependent on the FG. For a CLV disc, the FG is read and the spindle error undergoes PWM (Pulse Width Modulation) by the chopper to change the gain. This is to obtain the spindle gain that corresponds to the rpm. The 8-inch disc's gain also switches the chopper according to the commands from the microcomputer.

Since IC901 is not compatible with the CDV disc's gain, an externally attached Q906 Tr switch is used for the switching. The switch between pins 29 and 30 of IC901 is the chopper switch. This chopper is attached to the spindle loop's last step. Therefore, since chopping is done up to the direct current error voltage (the voltage which rotates the spindle motor), the dynamic range at the outer periphery of the CLV disc will become inadequate. As a result, the direct current error voltage is bypassed by LPF2 to prevent offset.

4. 4 TBC Signal Flow

The TBC (Time Base Corrector) signal flow is described as follows. The quartz oscillator at pins 9 and 10 of IC901 produces a standard frequency of 14.31818 MHz. After 1/910 division, the REF-H is output to pin 8 and input to pin 37. The C-SYNC that is input to pin 36 undergoes dropout protection and becomes PB-H. Both signals are input to the PFC (Phase Frequency Comparator) and output from pin 17. Then they are smoothed by the C933 capacitor. After they pass through the buffer amplifier, the H error is output from pin 18. Meanwhile, the video signal whose chroma component had been removed by the BPF is input to pin 15 and undergoes waveform shaping by the limiter. Then the REF-SC (Reference Sub-carrier) which divided 14.31818 MHz into four undergoes phase comparison (EXOR circuit) and passes through the burst gate.

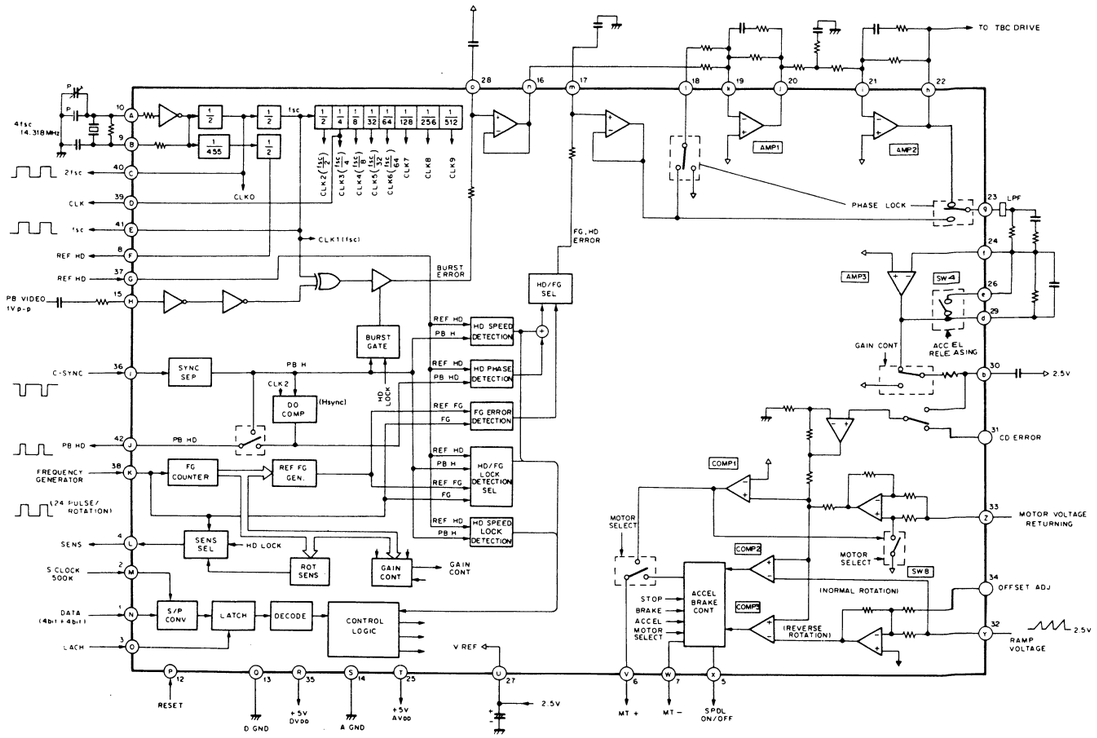
Next, the signal is smoothed by the C909 capacitor (IC901 pin 20) and it passes through the buffer amplifier. Then it is output from pin 16 as a burst error. The H error passes through EQ1 and the burst error passes through EQ2. Then they are mixed by AMP1. After passing through EQ3, EQ 4, and EQ5, it passes through IC902(1/2) and drives the CCD. IC901 operates while centering on an operation point of 2.5V of the built-in OP AMP. Whereas IC902(1/2) operates while centering on 0V. The CCD loop consists of EQ1 to EQ5 above.

In the CCD loop, the direct current error for the spindle servo has more control. Therefore this direct current component controls the spindle motor's rpm. The FG loop or H loop is selected by the switch between pins 22 and 23 of IC901. Then it is input to LPF1. The LPF1 removes the FG error's ripple. After passing through the IC902(2/2) buffer, it enters EQ7 and EQ8. Then it undergoes gain control by the chopper switch and it enters the PWM circuit. Pin 32 of IC902 is input with the RAMP signal that is produced by REF-H. The spindle error undergoes PWM(Pulse Width Modulation). Then it passes through the Q203 to Q206 switching drivers (in the power supply board assembly) and drives the spindle motor. The PWM circuit is built-in in IC901. The remaining jitter component which could not be removed by the TBC is suppressed by the VPS(in the video block) as with previous player models.

The player does not execute the 140 nS shift with TBC for every jump as previous models did. The reason is that since the loop relies on the burst error, it will be led into the 140 nS shifted phase for every jump in a short time. In order to make the lead-in smoother, the burst error is held by Q910 and C934 before and after the jump. Also, the ripple component of the burst error generated in IC901 may cause color irregularity. Therefore, with C-SYNC, Q910 does sample hold to suppress the ripple component.

These IC901 operations are controlled by the serial data from the microcomputer. From when the power is turned on to when the initial setting is completed by the microcomputer, D904 and D905 prevent the PWM circuit's output pins 6 and 7 from becoming high and also prevent all the spindle driver's (on the power supply board Ass'y) transistors from turning ON.

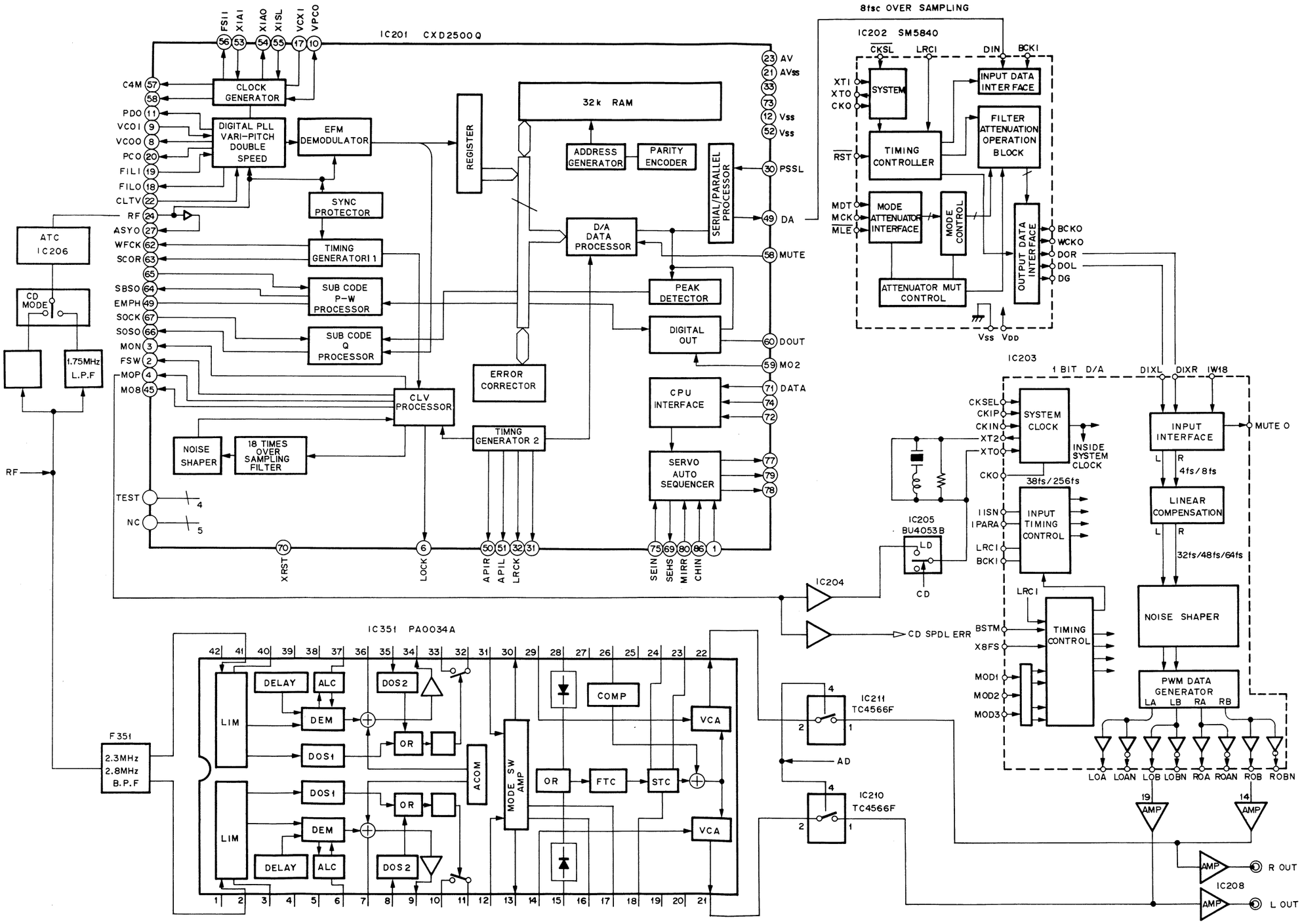
HD49403NT Internal Block Diagram



HD49403NT Pin Description

PIN No.	SYMBOL	I/O	DESCRIPTION
1	SDAT	I	Serial data input from CPU.
2	SCLK		Serial data clock input from CPU. Strobed at the negative edge.
3	LACH		Serial data latch pulse input from CPU.
4	SENS	O	IC internal state sense output. High-impedance when not selected.
5	STOP		Spindle motor ON signal output.
6	MTPL		Spindle motor accelerating signal output(brush motor). Torque generation direction signal output (3-phase).
7	MTMI		Spindle motor decelerating signal output(brush motor). Torque generation signal output(2-phase).
8	RHDO		Reference HD signal output.
9	OSCO		4 fsc reference signal output.
10	OSCI	I	4 fsc reference signal input.
11	TEST		Test pin (0V).
12	RSET		System reset signal input. "L"=reset.
13	DGND	-	GND for digital circuits (0V).
14	AGND		GND for analog circuits (0V).
15	PBVI	I	Burst signal input (AC-coupled).
16	AP1O	O	Op-amp 1 output (burst signal time-axis error output).
17	PFDO		LPF capacitor pin for HD/FG signal time-axis error smoothing.
18	AP2O		Op-amp 2 output (burst signal time-axis error output).
19	AP3I	I	Op-amp 3 invert input.
20	AP3O	O	Op-amp 3 invert output.
21	AP4I	I	Op-amp 4 invert input.
22	AP4O	O	Op-amp 4 output (for CCD circuit phase compensation).
23	SW3O		Analog switch 3 output (HD/FG control select).
24	AP5I	I	Op-amp 5 invert input
25	AVDD	-	Power supply for analog circuits (5V).
26	SW4I	I	Analog switch 4(to discharge capacitor).
27	VREF	-	Reference power supply(Op-amp reference voltage: 2.5V).
28	BUER	O	LPF capacitor pin for burst signal time-axis error smoothing.
29	AP5O		Op-amp 5 output(for phase compensation of spindle motor circuits).
30	LPFC	-	LPF capacitor pin for gain control.
31	CDER	I	CD mode spindle motor control signal input.
32	VRMP		Lamp signal input for PWM.
33	VMOT		Spindle motor pin voltage feedback input
34	OFAD		Op-amp offset adjustment input.
35	DVDD	-	Power supply for digital circuits (5V).
36	SYNC	I	Composite sync signal input (digital signal).
37	RHDI		Reference HD signal input. Normally connected to RHDO(pin 8).
38	FG		FG input(digital signal).
39	CLK	O	Clock signal output for FTS.(447kHz)
40	2FSC		2 fsc clock signal output.
41	FSC		fsc clock signal output.
42	PBHD		Playback HD signal output(after dropout compensation).

AUDIO SIGNAL BLOCK DIAGRAM



5. AUDIO SIGNAL DESCRIPTION

5. 1 Analog Audio System Description (AFM section)

1) PA0034 Description

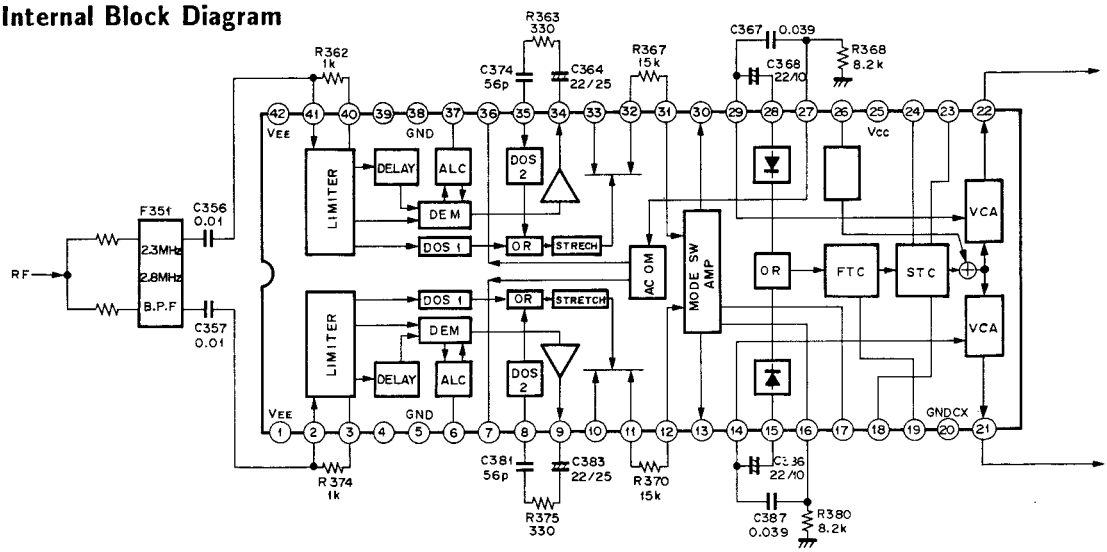
After the audio FM signal which was removed from the 2.3MHz (Lch) and the 2.8MHz (Rch) band-pass filters is demodulated, it will pass through the front hold circuit, the de-emphasis circuit, and the VCA (Voltage Control Amplifier). Then it is output as analog audio. Any dropout will be detected by the dropout detector. During the dropout detection, the front hold circuit will maintain the signal level at the level immediately before the dropout was produced. This is to prevent noise.

Also, the CX noise reduction system expands the audio circuit's dynamic range and improves the S/N ratio.

PA0034 is a single-chip IC dedicated to LD audio. It performs all of the signal processing above.

The analog audio L and R signals output from pins 22 and 21 are sent to the output terminals after digital or analog is selected by the IC210 and IC211 (TC4566F) switching ICs.

PA0034 Internal Block Diagram



PA0034 Pin Description

PIN No.	SYMBOL	Terminal Function	PIN No.	SYMBOL	Terminal Function
1	VEER	Power supply input	22	LOUT	Lch output
2	VINR	FM signal input	23	STC2	STC terminal 2
3	BIASR	Input bias	24	STC1	STC terminal 1
4	VREFR	Internal reference power supply	25	VCC	Power supply input
5	GNDR	GND	26	COMP	Compensator terminal
6	ALCR	ALC capacitor	27	TBC	TBC error signal input
7	CSR	Carrier deletion	28	CINL	CX control signal input
8	DOS2R	DOS2 input	29	CXINL	CX input
9	DEMOR	Demodulator output	30	SWOL	Mode select amp output
10	SINR	Dropout correction switch input	31	SWINL	Mode select amp input
11	DOCR	Dropout correction switch output	32	DOCL	Dropout correction switch output
12	SWINR	Mode select amp input	33	SINL	Dropout correction switch input
13	SWOR	Mode select amp output	34	DEMOL	Demodulator output
14	CXINR	CX input	35	DOS2L	DOS2 input
15	CINR	CX control signal input	36	CSL	Carrier deletion
16	R	Mode select port R	37	ALCL	ALC capacitor
17	L	Mode select port L	38	GNDL	GND
18	CX	CX control	39	VREFL	Internal reference power supply
19	FTC	Capacitor connection for FTC	40	BIASL	Input bias
20	GNDCX	GND	41	VINL	FM signal input
21	ROUT	Rch output	42	VEEL	Power supply input

5. 2 Digital Audio Circuit Outline (DSP section)

1) Outline

The RF signal from the FTS section passes through the 1.75MHz low-pass filter. The low frequency of the separated EFM signal (which boosts during recording) is flattened by the de-emphasis circuit. Then the pulse is formed by the ATC (Automatic Threshold Control) of IC206(TC74HCU04 AP) and input to pin 24 of IC201 (CXD2500).

The address of the storage RAM is controlled by the frame synchronizing signal that is separated from data and the clock reproduced by the PLL from the EFM signal that was demodulated by. CXD2500. The audio data stored in RAM must be read according to an accurate and stable clock. Otherwise the audio signal played back will have jitter or wow/flutter. Also, if the RAM is written to and read by an unrelated clock, the RAM will become full. The quartz oscillator's output, which is synchronized with the playback EFM signal's average frequency, is therefore used as the reading clock.

CXD2500 output pin 34's digital audio signal passes through the IC202(SM5840AP) 8fs oversampling digital filter. After undergoing digital/analog conversion by IC203 (SM5860BF), the signal is amplified by IC208 and IC209 and output.

2) CXD2500 Features

The CXD2500 has the following features :

1. Better frame sync protection

The sync protection window is produced by the X'tal circuit which has no bit slip. A protection window is also inserted before and after the sync protection window.

2. 4-layer correction

There is 4-layer correction for the error correction. The correction capacity for the burst error has been doubled to 16 frames.

3. Interleave error protection

This prevents noise for non-consecutive frames.

4. Built-in 32K RAM

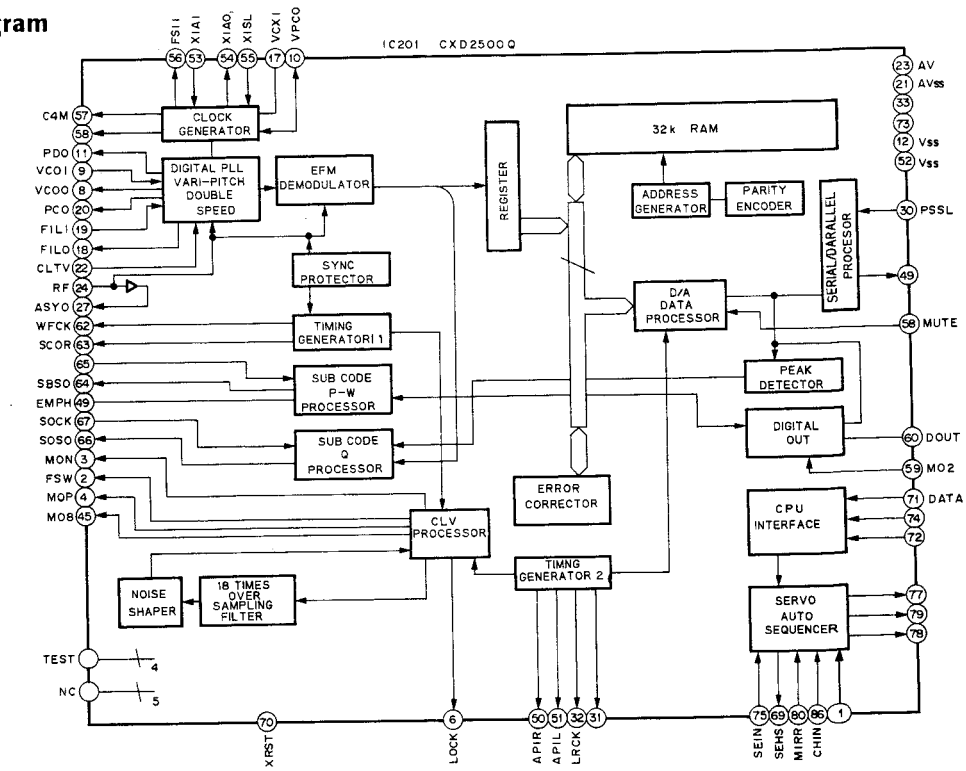
5. Digital peak meter and level meter functions

6. Variable pitch playback

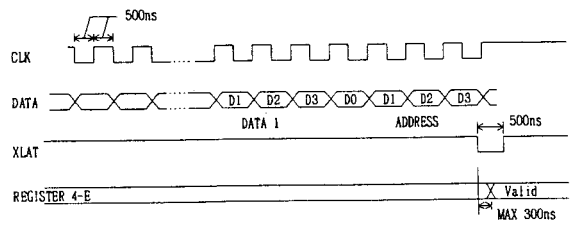
The PLL's output clock on the master side can be varied.

7. Auto zero cross mute

CXD2500Q Internal Block Diagram



Interface Timing Chart



CXD2500Q Pin Description

PIN No.	SYMBOL	I/O		DESCRIPTION
1	FCOK		I	Focus OK input terminal. This is used for the SENS output and the servo auto sequencer.
2	FSW	O	Z 0	Spindle motor's output filter switching output.
3	MON	O	1 0	Spindle motor's ON-OFF control output.
4	MDP	O	1 Z 0	Spindle motor's servo control.
5	MDS	O	1 Z 0	Spindle motor's servo control.
6	LOCK	O	1 0	H output when GFS undergoes sampling LH at 460 Hz. L output when there is L eight consecutive times.
7	NC			
8	VCOO	O	1 0	Oscillation circuit output for the analog EFM PLL.
9	VCOi		I	Oscillation circuit input fLOCK =8.6436 MHz for the analog EFM PLL
10	TEST		I	TEST pin. Normally GND.
11	PDO	O	1 Z 0	Charge pump output for the analog EFM PLL.
12	Vss			GND
13 14 15	NC			
16	VPCO	O	1 Z 0	PLL charge pump output for variable pitch.
17	VCKi		I	Clock input fc center =16.9344MHz from the variable pitch external VCO.
18	Filo	O	A	Filter output (analog) for master PLL (slave = digital PLL).
19	FiLi		I	Filter input for the master PLL.
20	PCO	O	1 Z 0	Charge pump output for the master PLL.
21	AVss			Analog GND.
22	CLTV		I	VCO control voltage input for the master PLL.
23	AVDD			Analog power supply (+5 V).
24	RF		I	EFM input after asymmetry correction.
25	TEST		I	To be GND.
26	TEST		I	To be GND.
27	ASYO	O	1 0	EFM full-swing output.
28	TEST		I	To be GND.
29	NC			
30	PSSL		I	Audio data output mode switching input. "L" serial output. Parallel output with "H" .
31	WDCK	O	1 0	D/A interface for the 48-bit slot. Word clock f = 2Fs.
32	LRCK	O	1 0	D/A interface for the 48-bit slot. LR clock f = Fs.
33	VDD			Power supply (+5V)
34	DA16	O	1 0	DA16 (MSB) output when PSSL = 1. 48 slot serial data (2S'COMP) when PSSL = 0.
35	DA15	O	1 0	DA15 output when PSSL = 1. 48-bit slot bit clock when PSSL = 0.
36	DA14	O	1 0	DA14 output when PSSL = 1. 64-bit slot serial data 2S'COMP LSB first when PSSL = 0.
37	DA13	O	1 0	DA13 output when PSSL = 1. 64-bit slot bit clock when PSSL = 0.
38	DA12	O	1 0	DA12 output when PSSL = 1. 64-bit slot and LR clock when PSSL = 0.
39	DA11	O	1 0	DA11 output when PSSL = 1. GTOP output when PSSL = 0.
40	DA10	O	1 0	DA10 output when PSSL = 1. XUGF output when PSSL = 0.

PIN No.	SYMBOL	I/O		DESCRIPTION
41	DA09	O	1 0	DA10 output when PSSL = 1. XPLCK output when PSSL = 0.
42	DA08	O	1 0	DA08 output when PSSL = 1. GFS output when PSSL = 0.
43	DA07	O	1 0	DA07 output when PSSL = 1. RFCK output when PSSL = 0.
44	DA06	O	1 0	DA06 output when PSSL = 1. C2PO output when PSSL = 0.
45	DA05	O	1 0	DA05 output when PSSL = 1. XRAOF output when PSSL = 0.
46	DA04	O	1 0	DA04 output when PSSL = 1. MNT3 output when PSSL = 0.
47	DA03	O	1 0	DA03 output when PSSL = 1. MNT2 output when PSSL = 0.
48	DA02	O	1 0	DA02 output when PSSL = 1. MNT1 output when PSSL = 0.
49	DA01	O	1 0	DA01 output when PSSL = 1. MNT0 output when PSSL = 0.
50	APTR	O	1 0	Aperture correction control output. "H" for the R ch.
51	APTL	O	1 0	Aperture correction control output. "H" for the L ch.
52	Vss			GND
53	XTAi	I		16.9344 MHz or 33.8688 MHz Xtal oscillation circuit input.
54	XTAO	O	1 0	16.9344 MHz or 33.8688 MHz Xtal oscillation circuit output.
55	XTSL	I		Xtal selection input terminal. "L"when it is 16.9344 MHz. "H" when it is 33.8688 MHz.
56	FSTT	O	1 0	2/3 divided output of the Xtal oscillation. Fixed during variable pitch.
57	C4M	O	1 0	4.2336 MHz output. Changes during variable pitch.
58	C16M	O	1 0	19.9344 MHz output. Changes during variable pitch.
59	MD2	I		Digital OUT ON/OFF control. ON when "H" , and OFF when "L".
60	DOUT	O	1 0	Digital OUT output terminal.
61	EMPH	O	1 0	"H" output when the playback disc has emphasis. "L"output when it has no emphasis.
62	WFCK	O	1 0	Write frame clock output.
63	SCOR	O	1 0	"H" output when the subcode sync SO or SI is detected.
64	SBSO	O	1 0	Sub P - W code and serial output.
65	EXCK	I		For SBSO lead out. External clock input.
66	SQSO	O	1 0	SubQ 80-bit and PCM peak data 16-bit output.
67	SQCK	I		External clock input for SQSO lead out.
68	MUTE	I		Mute with "H" , and cancel with "L".
69	SENS	O	1 0	SENS output. Sent to the CPU.
70	XRST	I		System reset. Reset when "L".
71	DATA	I		Serial data input from the CPU.
72	XLAT	I		Serial data from the CPU is latched with the latch input shutdown.
73	VDD			Power supply input (+5V).
74	CLK	I		From the CPU, serial data transfer clock input.
75	SEIN	I		From the SSP, SENSE input.
76	CNiN	I		Track jump count signal input.
77	DATO	O	1 0	Serial data output to the SSP.
78	XLTO	O	1 0	Serial data latch output to the SSP. Latched during shutdown.
79	CLKO	O	1 0	SP serial data transfer clock output.
80	MiRR	I		Mirror signal input. Used with the auto sequencer for jumps exceeding 128 tracks.

3) CXD2500 Command Code

As shown in the following table, the CXD2500 has 4-bit registers which have addresses from 4 to E. These registers are operated by being input externally with a total of 8 bits (address + data) of data.

CXD2500 Instruction and RESET Initialization

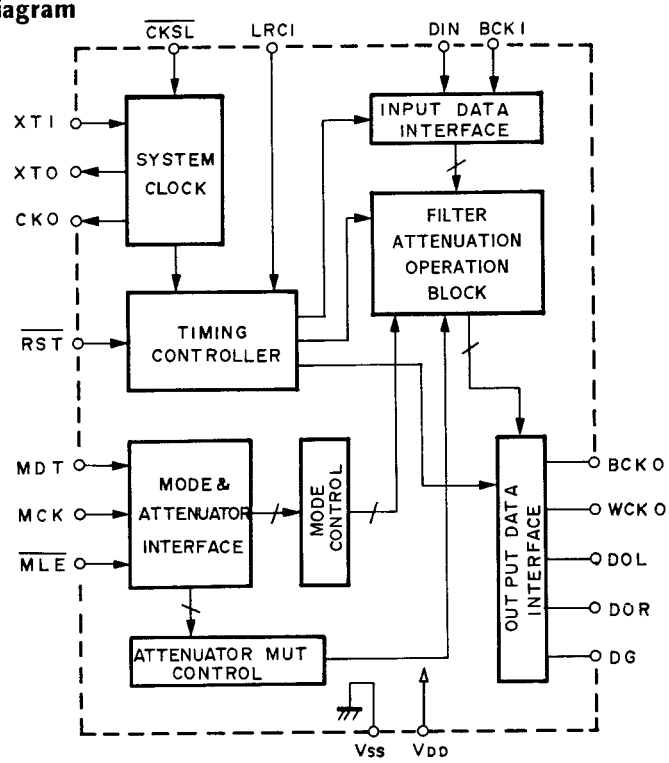
registers Name	Commands	Address				Data1				Data2				Data3				Data4			
		D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
4	Auto Sequence	0	1	0	0	AS3	AS2	AS1	AS0	—	—	—	—	—	—	—	—	—	—	—	—
5	Blind(A,E), Overflow(C) Brake(A)	0	1	0	1	0.18ms 0.36ms	0.09ms 0.18ms	0.045ms 0.09ms	0.022ms 0.045ms	—	—	—	—	—	—	—	—	—	—	—	—
6	KICK(D)	0	1	1	0	11.6ms	5.8ms	2.9ms	1.45ms	—	—	—	—	—	—	—	—	—	—	—	—
7	Auto Sequencer(N) Track Jump	0	1	1	1	32,768	16,384	8,192	4,096	2,048	1,024	512	256	128	64	32	16	8	4	2	1
8	MODE	1	0	0	0	CDROM	0	D OUT MuTu-F	WSEL	—	—	—	—	—	—	—	—	—	—	—	—
9	Function	1	0	0	1	D CLV ON-OFF	DSPB ON-OFF	A SEQ ON-OFF	D PLL ON-OFF	Bili GL MAIN	Bili GL SUB	—	—	—	—	—	—	—	—	—	—
A	Audio CTRL	1	0	1	0	Vari UP	Vari Down	MUTE	ATT	PCT1	PCT2	—	—	—	—	—	—	—	—	—	—
B	Traverse Monitor Counter	1	0	1	1	32,768	16,384	8,192	4,096	2,048	1,024	512	256	128	64	32	16	8	4	2	1
C	Servo Factor	1	1	0	0	Gain MDPI	Gain MDPO	Gain MOSI	Gain MOSO	—	—	—	—	—	—	—	—	—	—	—	—
D	CLV CTRL	1	1	0	1	DCLV PWM MD	TB	TP	CLVS Gain	—	—	—	—	—	—	—	—	—	—	—	—
E	CLV MODE	1	1	1	0	CH3	CH2	CH1	CH0	—	—	—	—	—	—	—	—	—	—	—	—

4	Auto Sequence	0	1	0	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
5	Blind(A,E), Overflow(C) Brake(A)	0	1	0	1	0	1	0	1	—	—	—	—	—	—	—	—	—	—	—	—
6	KICK(D)	0	1	1	0	0	1	1	1	—	—	—	—	—	—	—	—	—	—	—	—
7	Auto Sequencer($\dot{N}$) Track Jump	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
8	MODE	1	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
9	Function	1	0	0	1	1	0	0	1	0	0	$\underline{0}$	—	—	—	—	—	—	—	—	—
A	Audio CTRL	1	0	1	0	0	0	1	1	0	0	—	—	—	—	—	—	—	—	—	—
B	Traverse Monitor Counter	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C	Servo Factor	1	1	0	0	0	1	1	0	—	—	—	—	—	—	—	—	—	—	—	—
D	CLV CTRL	1	1	0	1	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
E	CLV MODE	1	1	1	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—

4) SM5840

DA01 to DA16, which are output from pin 49 of CXD2500, are input to pin 18 of SM5840. SM5840 is a multi-function digital filter for 8fs oversampling. Its functions include digital emphasis, digital attenuation, and soft muting.

SM5840 Internal Block Diagram

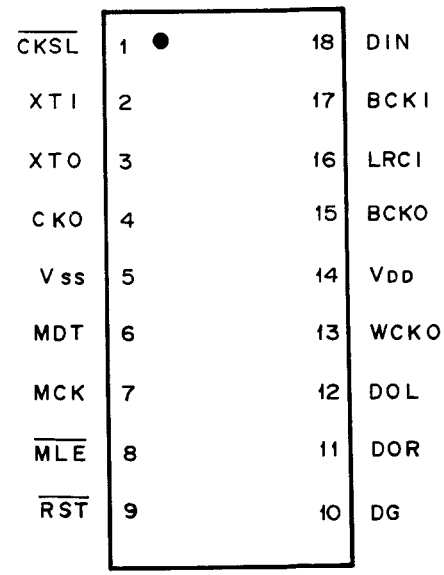


SM5840 Pin Description

"fs" means sampling frequency of input data.

PIN No.	SYMBOL	I/O	Description	
1	CKSL	IP	Select frequency of OSC and input (When CKSL=E, 384fs)	
2	XTI	I	OSC input (Frequency selected by CKSL)	
3	XTO	O	OSC output	
4	CKO	O	Clock of OSC output (Frequency is same as XTI)	
5	Vss		GND	
6	MDT	IP	Mode setting data	Setting the digital attenuator and the mode flag register.
7	MCK	IP	Mode setting clock	
8	MLE	IP	Mode setting latch enable	
9	RST	IP	System reset (Initialize)	
10	DG	O	When 8fsLR parallel output mode; Output De-glitch	
11	DOR	O	When 8fsLR parallel output mode; Output Rch data	
12	DOL	O	When 8fsLR parallel output mode; Output Lch data	
13	WCKO	O	Clock for output words	
14	VDD		Power supply input (5V)	
15	BCKO	O	Clock for output bits	
16	LRCI	IP	Clock for sampling rate (fs) of input data	
17	BCKI	IP	Clock for input bits	
18	DIN	IP	Data input	

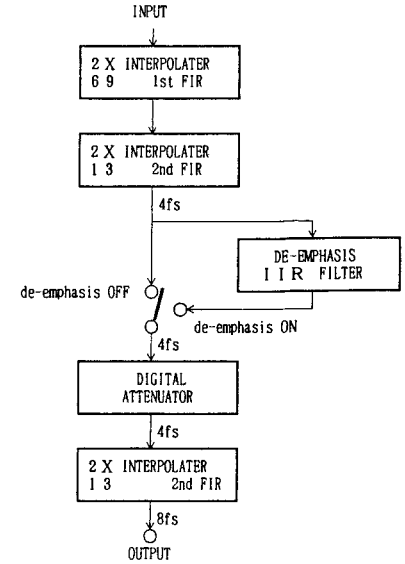
SM5840 External View



SM5840's basic computation block is shown on the right. The interpolation computation block consists of doubled interpolation filters connected in three steps. It outputs 8fs oversampling data for the signal that is input at the fs sample rate.

The output data is an 18 bit MSB first 2's complement. It is output from pins 11 and 12. With the 8fsc L and R parallel output mode, the L and R channel outputs are output simultaneously from two output terminals.

The input data is input from pin 18 in 16 bits, MSB first serial, and two's complement. All the serial data bits are read to the SIPO register (serial/parallel conversion register) with the bit clock BCKI's startup edge and are converted to parallel data. The SIPO's output is transferred to the respective L ch and R ch input registers with the LRCI clock's shutdown/startup edge.



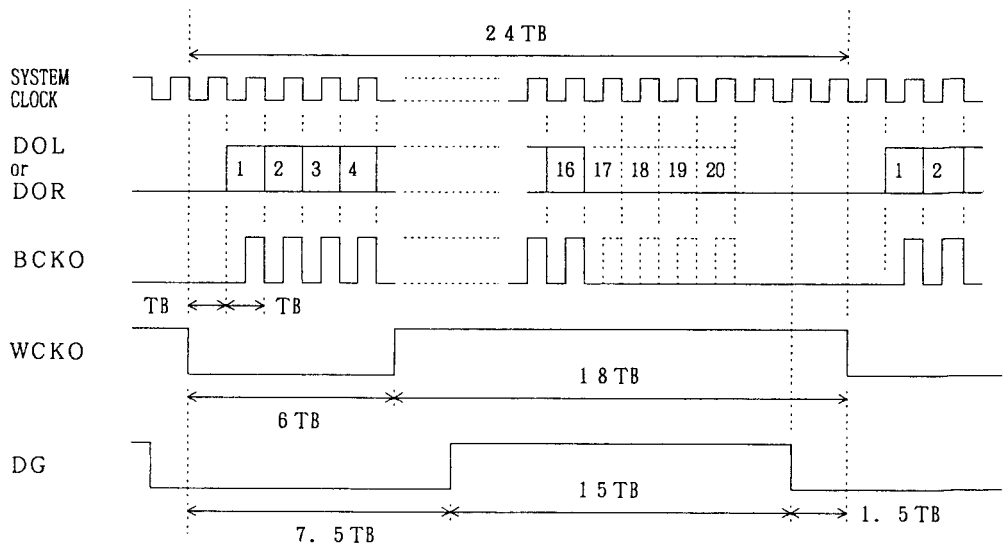


Fig. Data Output Timing Chart

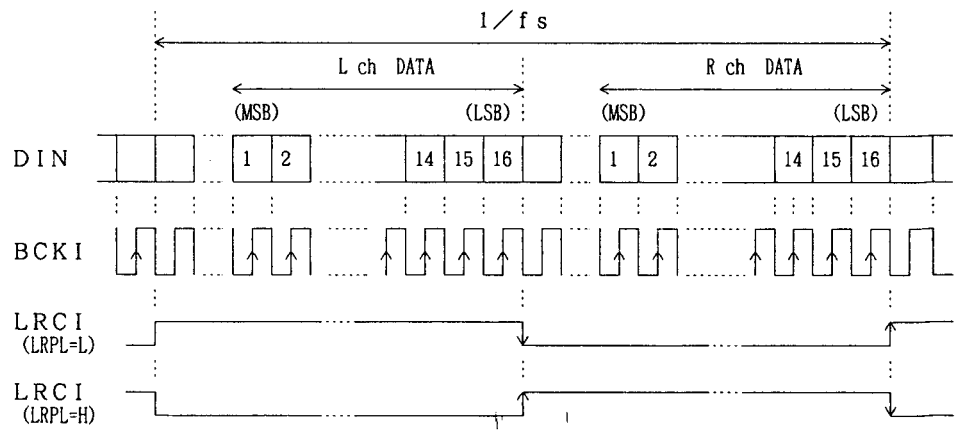
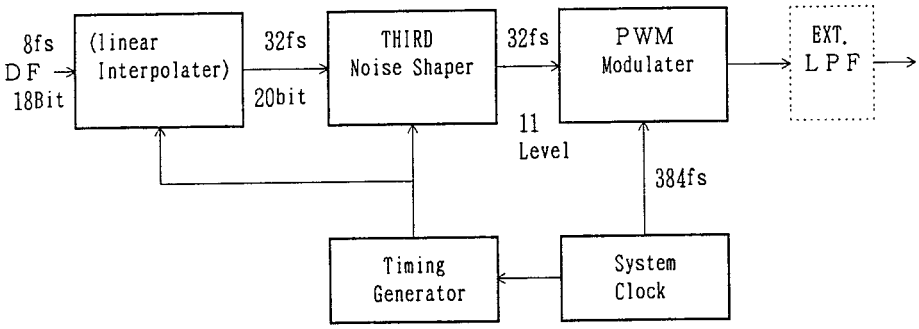


Fig. Data Input Timing Chart

5) SM5860

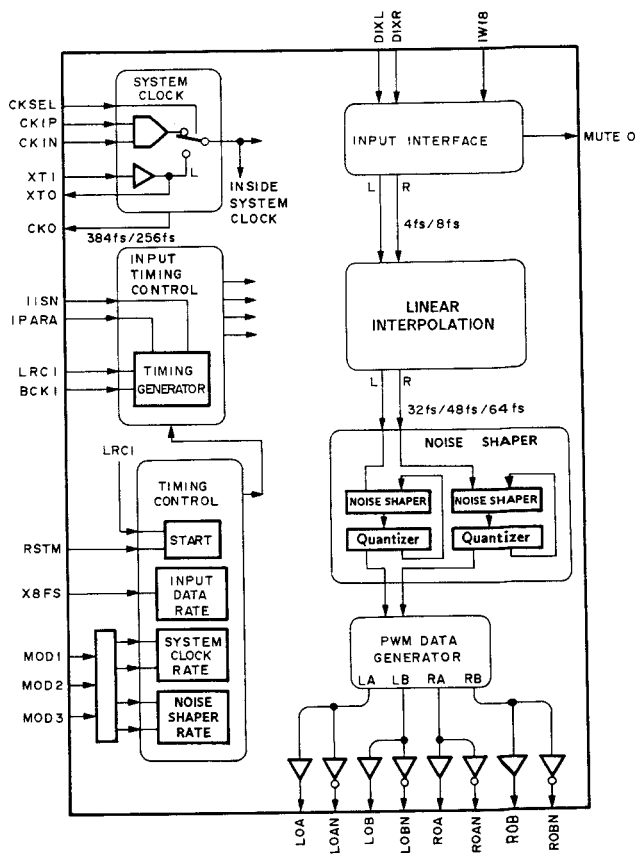
The data that is output from pins 11 and 12 of SM5840 is input to pins 40 and 41 of SM5860. SM5860 is a D/A converter for the 18-bit input. It has the following features :

- Built-in D/A converter for the LR2 channel.
- Built-in overflow limiter.
- Built-in quartz oscillation circuit.
- I/O TTL compatible.

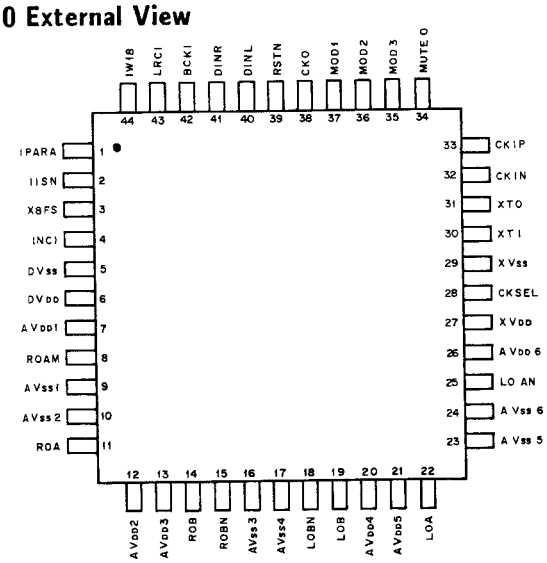


The SM5860's internal block is shown in the figure.
The linear interpolator receives the data from SM5840.
There is a 20-bit output resolution with the section of data which underwent higher order (32 fs) oversampling by the linear interpolation. With the linear interpolator, the next step's noise shaper shows the signal's (oversampled by the linear interpolator) 2^{20} line resolution signal with the level 11's signal. This method thereby pushes out the re-quantized noise from the audio band.
To output the data that was dropped from the 20 bit to level 11 by the noise shaper, the PWM modulator is used.
For the level number increase, the PWM modulation allows an increase of 1 system clock time toward only one side of the sample period center. A 1-bit D/A converter which uses low crystal oscillation is thereby realized.

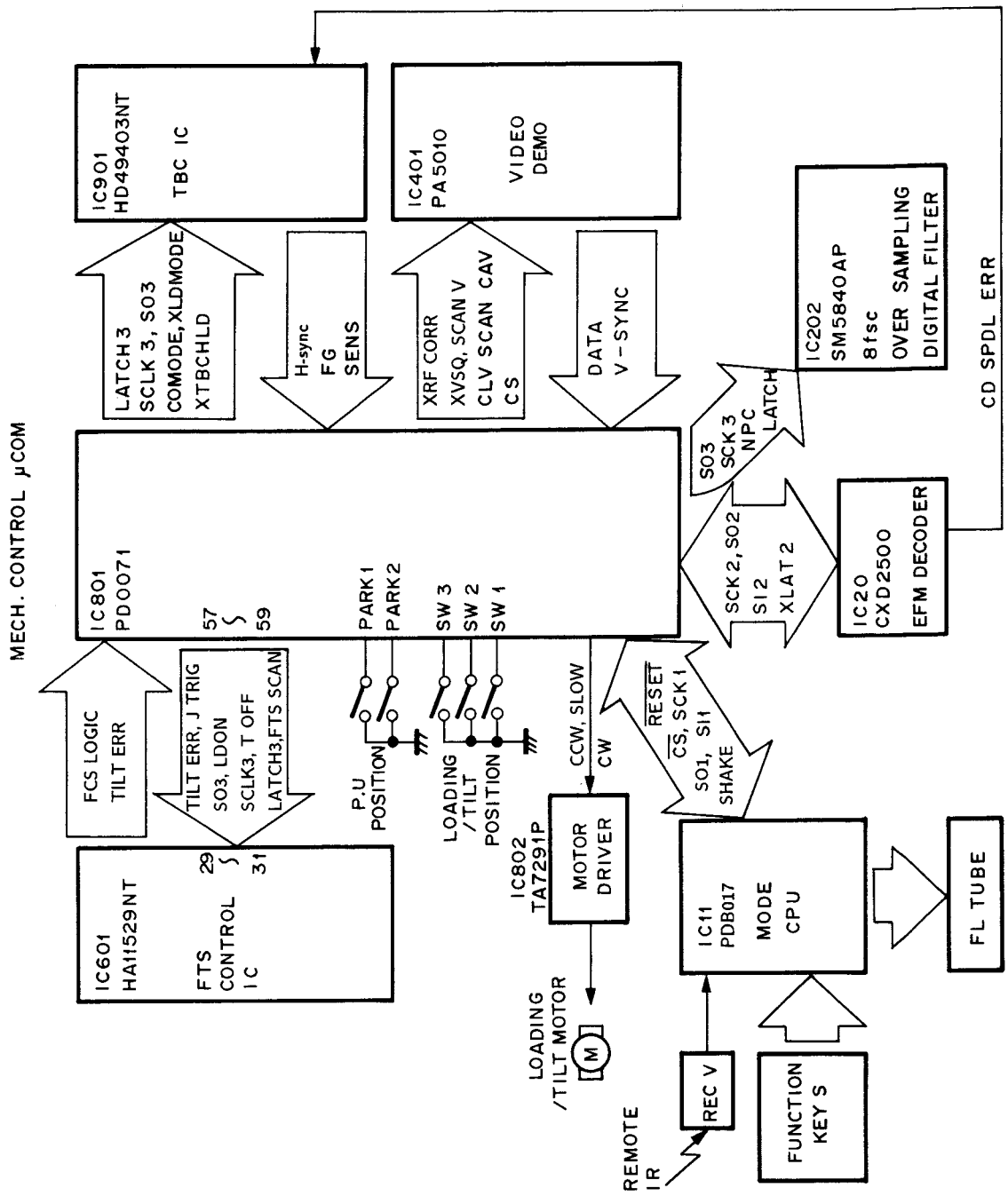
SM5860 Internal Block Diagram



SM5860 External View



CONTROL SYSTEM BLOCK DIAGRAM

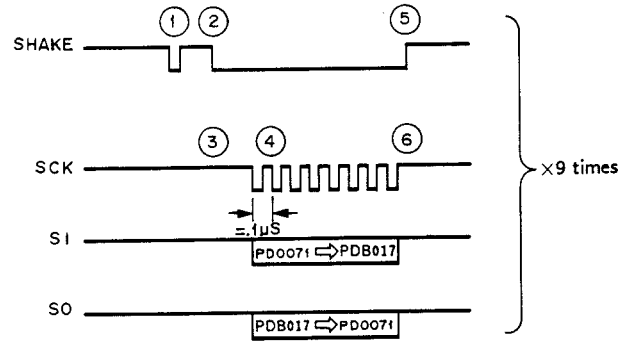


6 Control System

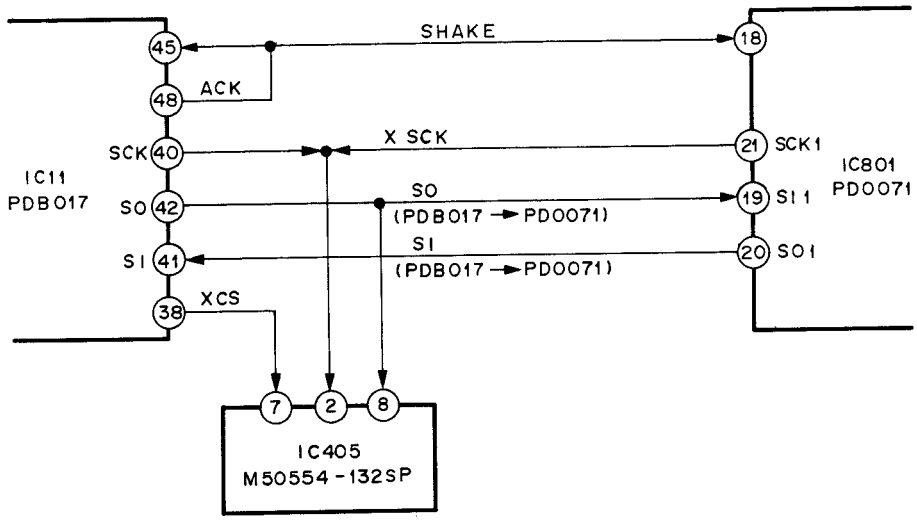
6. 1 Microcomputer interfaces

The player's microcomputer consists of two chips : an 8-bit microcomputer (IC801 : PD0071) which controls the mechanisms and a 4-bit microcomputer (IC11 : PDB017) which controls the operation and display. These two microcomputers are connected via a serial interface. This transmission line is also used for controlling the character generator IC (IC405 : M50554-132SP).

● Timing Chart of Microcomputers' Communication



● Serial Data Transfer Connection



● Microcomputer communication sequence

1. PD0071 sets the SHAKE terminal (pin 18) to"L"for several μS to request the start of a communication with PDB017.
2. When PDB017 receives the communication start request, it sets the ACK terminal (pin 48) to"L"and informs PD 0071 that communication has been enabled.
3. PD0071 then sets SCK1 (pin 21), which had been used as an input port, to the output mode. PDB017 sets SCK (pin 40) to the input mode and connects the communication line between the microcomputers.
4. PD0071 sends the transfer clock(1MHz) in 8 bits. The data is then sent and received in synchronization with this clock.
5. When PDB017 receives 8-bit data, it sets the ACK terminal (pin 48) to"H"and reports that a single communication is completed.
6. PD0071 set SCK1 (pin 21) to the input mode, and PDB017 sets SCK (pin 40) to the output mode. The communication line is thereby disconnected, and a single communication is completed.

★ The communication is takes place at a cycle between 10mS and 30mS. Nine bytes of data are transmitted at one time.

★ The handshake is done on a single line. Both PD0071 and PDB017 use a single port for both input and output. The output mode will be set only when the output is"L". Otherwise, it will be set to the input mode (high impedance). Also, before"L"is output, whether the SHAKE terminal is"H"is mutually checked. This is to prevent signal confusion between output signals.

★ The communication data is appended with a check code to prevent transfer errors. If sixteen consecutive transfer errors are detected, PDB017 will output the reset signal to PD0071 to reset it to the initial condition. This will also happen if the communication is not 300mS or longer.

6. 2 Mode Control Outline

Mode microcomputer (IC11 : PDB017)

The mode microcomputer performs the following :

1. Key data/remote control signal processing
   The key switch and remote control signals are received and processed for the specified keys.
2. FL display operation
   The FL tube display (VAW1010) is operated.
3. Screen display control
   The character generator IC(IC405 : M50554-132SP) is controlled and characters are superimposed on the screen. The blue back is also controlled.
4. Mechanism control micro computer control
   When operational instructions are given to the mechanism control microcomputer(IC801 : PD0071), the time data is read at the same time.
5. System reset management
   If there is any communication problems with the mechanism control microcomputer, the system reset will be activated to return the unit to the initial condition.

PIN No.	SYMBOL	I/O	DESCRIPTION
1	VDD	I	Power supply input (5V)
2			No connection
3			
4			
5			
6			
7	G1	O	FL lighting timing output "H": ON, "L": OFF
8	G2		
9	G3		
10	G4		
11	G5		
12	G6		
13	G7		
14	G8		
15	G9		
16	G10		
17	G11		
18	VDISP	I	FL display power supply input (−30V)
19	l	O	FL lighting segment output "H": ON, "L": OFF
20	k		
21	j		
22	i		
23	h		
24	g		
25	f		
26	e		
27	d		
28	c		
29	b		
30	a		
31	LAST MEMORY	O	LED lighting output. "H": ON, "L": OFF
32	CD DIRECT		

PIN No.	SYMBOL	I/O	DESCRIPTION
33	DOOR SW	I	Door switch input. "H": ON, "L": OFF
34	SYNC IN		Synchronized REC control input
35	SYNC OUT	O	Synchronized REC control output
36	POWER ON		Power ON/OFF "H": ON, "L": OFF
37	X RESET		PD0071 reset
38	X CS		M50554 select
39			No connection
40	X SCK	I/O	Serial data transfer clock
41	SI	I	Serial data input
42	SO	O	Serial data output
43	RESET	I	Reset input
44	SEL IR		Remote control unit input
45	SHAKE		Serial communication start request input
46			No connection
47			
48	ACK	O	Serial communication acceptance output
49	KS0	O	Key scan output "H": ON, "L": OFF
50	KS1		
51	KS2		
52	KS3		
53	KS4		
54	KS5		
55	KS6		
56	KIN0	I	Key data input "H": ON, "L": OFF
57	KIN1		
58	KIN2		
59	KIN3		
60	X2		No connection
61	X1		GND (Not used.)
62	Vss	-	GND
63	OSC2	I	Oscillator (6.0MHz)
64	OSC1	O	

6. 3 Mechanism Control Outline

1 Processing during power ON

After the power is turned ON, the mechanism control microcomputer (IC801 : PD0071) will execute the initialization in the following sequence upon reset cancellation (pin 28 : H→L).

1. The internal RAM and port are initialized.
2. HA11529NT is initialized.
3. CXD2500 is initialized.
4. The tray position is detected.
5. HD49403 is initialized.
6. Communications with PDB017 is checked.
7. The pickup position is initialized.
8. The disc rotation stops.
9. The loading mode is initialized.

After all of the above initializations are completed, normal operation will begin.

2 Loading motor control

The loading motor drive is controlled by the signals output (via the motor driver IC[IC802]) from pins 49 to 51 of the CONT section's mechanism control IC (IC801). The voltage applied to the loading motor is switched by the control signal as follows.

SLOW	CW	CCW	LOAD M+	LOAD M−	Motor Operation
L	L	L	.....	.....	.....
L	L	H	0V	5V	Low-speed CCW rotation
L	H	L	5V	0V	Low-speed CW rotation
L	H	H	0V	0V	Short brake mode
H	L	L	Open	Open	Motor both-ends open mode
H	L	H	0V	11V	High-speed CCW rotation
H	H	L	11V	0V	High-speed CW rotation
H	H	H	.....	.....	.....

CW: Clockwise direction CCW: Counterclockwise direction

• Loading/Clamp operation

For the disc tray opening and closing, disc clamp operation, and stop operation, the motor is operated while the cam gear position is detected by the loading/tilt position detection switch which is connected to pins 62 to 64 of IC801. The motor will operate in the high-speed mode. Even after the operation is completed, the loading/tilt position detection switch constantly monitors the cam gear position while the latter is in the standby position and in the tilt neutral position. If the cam gear position shifts, the motor will be operated in the low-speed mode.

• Tilt servo operation

When an LD disc or a CDV disc (video part) is played back, the loading motor will be used for the tilt servo. In this mode, the motor will be operated in the low-speed mode. The loading motor drive for the tilt servo will be PWM. There is two-stage duty (high-speed duty 50%, low-speed duty 8%). The tilt servo operates the loading motor so that the voltage of input pin 12 (TILT ERR) of IC801 becomes 2.5V. During normal playback, the tilt servo's operating range will be as follows :

CAV disc (12-inch) : Frames 0 - 40999
(8-inch) : Frames 0 - 16999
CLV disc (12-inch) : 0 min. - 44 min. 59 sec.
(8-inch) : 0 min. - 13 min. 59 sec.
CDV disc(video part) : 0 min. 0 sec. - 0 min. 59 sec.
(Recording time > 3 min.)

If there is a problem with the disc or the tilt sensor circuit and the pickup inclination is ± 2% or more and the TILT terminal's input voltage is still not within the set range, the status of the mechanical switch will be detected and the loading motor will be stopped.

• Slider motor control

The slider motor drive is controlled by the signal that is output from pin 18 of the FTS servo IC (IC601) via IC606. The voltage applied to the slider motor is switched by the control signal from the mechanism control IC (IC801).
When the pickup position is moved compulsorily during disc recognition and startup, the motor is operated while the pickup position is detected by the park switch connected to pins 33 and 34 of IC801.

PD0071 Pin Description

Pin No.	SYMBOL	I/O	Description
1	Vcc	-	Power supply connection (+5V)
2	SQ2	O	Analog audio switching signal output terminal. Digital audio is controlled by IC201(CXD2500Q). (*1)
3	SQ1		
4	N.C.		Unused
5	N.C.		
6	X DIGITAL	O	Digital/analog audio switching signal output terminal. This signal switches the signal which is output to LINE OUT and HEADPHONE. When "H", analog audio. When "L", digital audio. (*1)
7	XLDP		RF modulator switching signal output terminal.
8	XCX		Analog audio CX noise reduction switching signal output terminal.
9	LDON		Laser diode ON/OFF control signal output terminal. When "H" Laser diode ON. When "L" Laser diode OFF.
10	MUTE		Audio system mute control signal output terminal. When "L", MUTE OFF. When "H", MUTE ON.
11	NPC LATCH		Digital filter IC (IC202: SM5840AP) control latch signal output terminal.
12	TILT ERR	I	Tilt sensor output signal input terminal. (Analog signal) The signal which amplified the tilt sensor output by 40dB to 50dB is input (0V - 5V). This signal undergoes A-D conversion and becomes the control input for the tilt servo. The loading motor is controlled so that the TILT input signal becomes 2.5V.
13	GFS		CD (EFM signal) frame lock signal input terminal. (IC201: Connected to pin 12 of CXD2500Q) When "H", OK. When "L", NG.
14	XLAT2	O	IC201 CXD2500Q control latch signal output terminal.
15	SI2	I	IC201 CXD2500Q subcode data input terminal
16	SO2	O	IC201 CXD2500Q control data output terminal.
17	SCK2		IC201 CXD2500Q control/subcode reading clock signal output terminal.
18	SHAKE	I/O	Mode Control IC (IC11: PDB017) data transmission handshake signal terminal. This terminal is a bidirectional data line. It transmits the timing for the data transfer after the respective microcomputer switches between the output or input mode. (*2)
19	SI1	I	Mode Control IC data transmission data I/O terminal. SCK1(pin 21) will be set to the input mode when there is no communications with the Mode Control IC.
20	SO1	O	
21	SCK1	I/O	
22	T.CROSS	O	Tracking error zero cross signal input terminal. This signal monitors the tracking error signal. During track count search, this signal is counted and the slider motor is controlled.
23	SCOR	I	Subcode sync signal input terminal. When this signal is "H", the subcode signal is input from I201(CXD2500Q). The disc's playback status is also monitored through the existence or non-existence of the signal.
24	SENS		IC901(HD49403) SPDL servo status monitor signal input terminal.
25	XTBCHLD	O	During TBC servo jump, it is the correction signal output terminal. During a special playback of CAV disc, the signal becomes "L" when there is track jumping. After V sync and a fixed time period, it becomes "H".
26	V-Sync	I	Playback vertical synchronization signal input terminal for LD/CDV. The IC basically operates while in synchronization with this signal. (Trailing edge input) During a special playback mode for a CAV, the signal is the standard for producing the jump timing. It is "L" during vertical synchronization.
27	CNVss	-	GND.
28	XRESET	I	Reset signal input terminal. When "L", RESET. When "H", Normal operation.
29	XIN		9MHz clock oscillation input terminal.
30	XOUT	O	9MHz clock oscillation output terminal.
31	N.C.		Unused
32	Vss	-	GND.

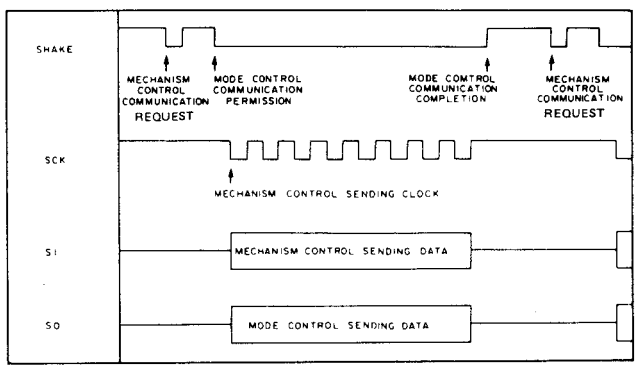
Pin No.	SYMBOL	I/O	Description
33	PARK2	I	The pickup position detection switch input terminals. Being a switch input for mechanism position detection, it detects the pickup's position. (*3)
34	PARK1		
35	FOCUS LOCK		Focus servo lock signal input terminal. It is used for focus servo lock detection. When "L", OK. When "H", NG.
36	1080/2080		Mechanism controller mode switching input terminal. When "H", CLD-1080.
37	FG		Spindle motor FG signal switching input terminal.
38	DATA		PHILIPS code decoder input terminal built-in in the mechanism controller.
39	Hsync		
40	Vsync		
41	CAV	O	CAV/CLV switching signal output terminal. (IC201: Connected to pin 17 of PA5010, it is used as the video NR switching signal.)
42	CLVSCAN		CLV V sync scan mode signal output terminal. When CLVSCAN is "L", SCANV(pin 44) is inserted to the video signal.
43	N.C.		Unused.
44	SCANV	O	Pseudo V sync signal output terminal for the CLV V sync scan.
45	XVSQ		Blue back switching signal output terminal for the video output. When "H", playback video. When "L", blue back.
46	XRFCORR		RF correction switching signal output terminal. (Connected to IC201 PA5010 pin 52.) "H" at the outer periphery of the CAV.
47	N.C.		Unused.
48	N.C.		
49	CCW	O	Loading/tilt motor rotational direction control signal output terminal. The motor's rotational direction and brake mode are selected by pins 49 and 50. Pin 49: counterclockwise. Pin 50: clockwise. (*4)
50	CW		
51	SLOW		Loading/tilt motor operation speed switching signal output terminal. When it is switched to the loading mode, high-speed operation will take effect. During tilt operation, low-speed operation will take effect. When, "L", low-speed. When "H", high-speed.
52	J. TRIG		Track jump signal output terminal.
53	FTSSCAN	I/O	Signal output terminal for tracking servo stabilization. Normally, it will be HI-Z in the input mode.
54	TOFF	O	Tracking servo operation control signal output terminal. This signal backs up the ON/OFF of the tracking servo operation. When "L", ON. When "H", OFF.
55	CD MODE		Servo equalizer switching signal output terminal. This is switched according to the disc to be played. (*5)
56	XLD MODE		
57	S03		Serial signal output terminal for the FTS servo IC(IC601: HA11529), the SPDL/TBC servo IC(IC901:HD49403), and the digital filter IC(IC202: SM5840AP). The serial signals of these three ICs are the same. They are distinguished by pin 11 (NPCLAT) and pin 59 (LATCH3).
58	SCLK3		
59	LATCH3		Latch signal output terminal for the FTS servo and the SPDL servo.
60	N.C.		Unused.
61	N.C.		
62	SW1	I	Loading/tilt position detection switch input terminals.
63	SW2		
64	SW3		

*1

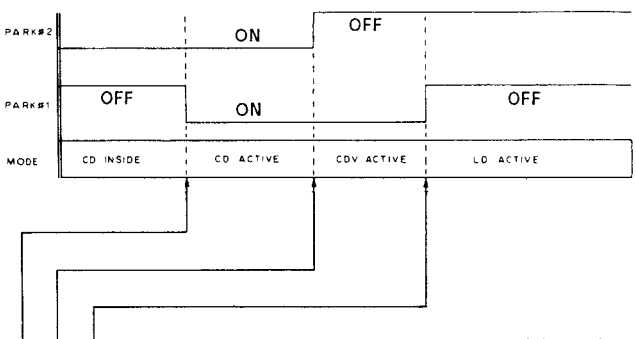
DIGITAL Pin 6	SQ1 Pin 3	SQ2 Pin 2	L-Ch Line Out	R-Ch Line Out
H	L	L	Analog L Channel	Analog R Channel
H	H	L	Analog L Channel	Analog L Channel
H	L	H	Analog R Channel	Analog R Channel
H	H	H	Mute	Mute
L	L	L	Digital L Channel	Digital R Channel
			Digital L Channel	Digital L Channel
			Digital R Channel	Digital R Channel
			Digital –12dB-L	Digital –12dB-R

CXD2500 switching the digital audio channel by commands from microcomputer.

*2



*3



LD-inside position: Indicating the start of the active program area of an LD disc (R55 – R56.4)

CDV-inside position: Indicating the start of the video part of a CDV disc. (R37 – R38.4)

CD-inside position: Indicating the start of the active program of a CD disc. (R25 – R26.4)

R: The distance from center of the spindle motor.

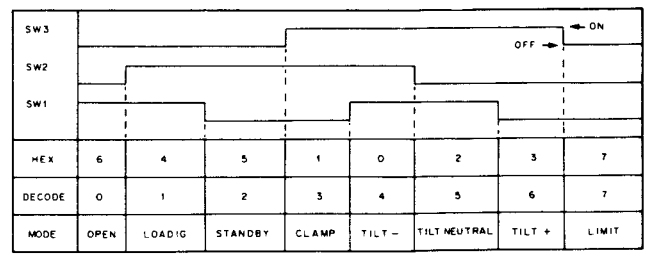
*4

CW	CCW	Loading/Tilt Motor Operation
L	L	Motor both-ends release (open mode)
L	H	Loading-out direction rotation
H	L	Loading-in direction rotation
H	H	Motor both-ends short-circuit (short-circuit mode)

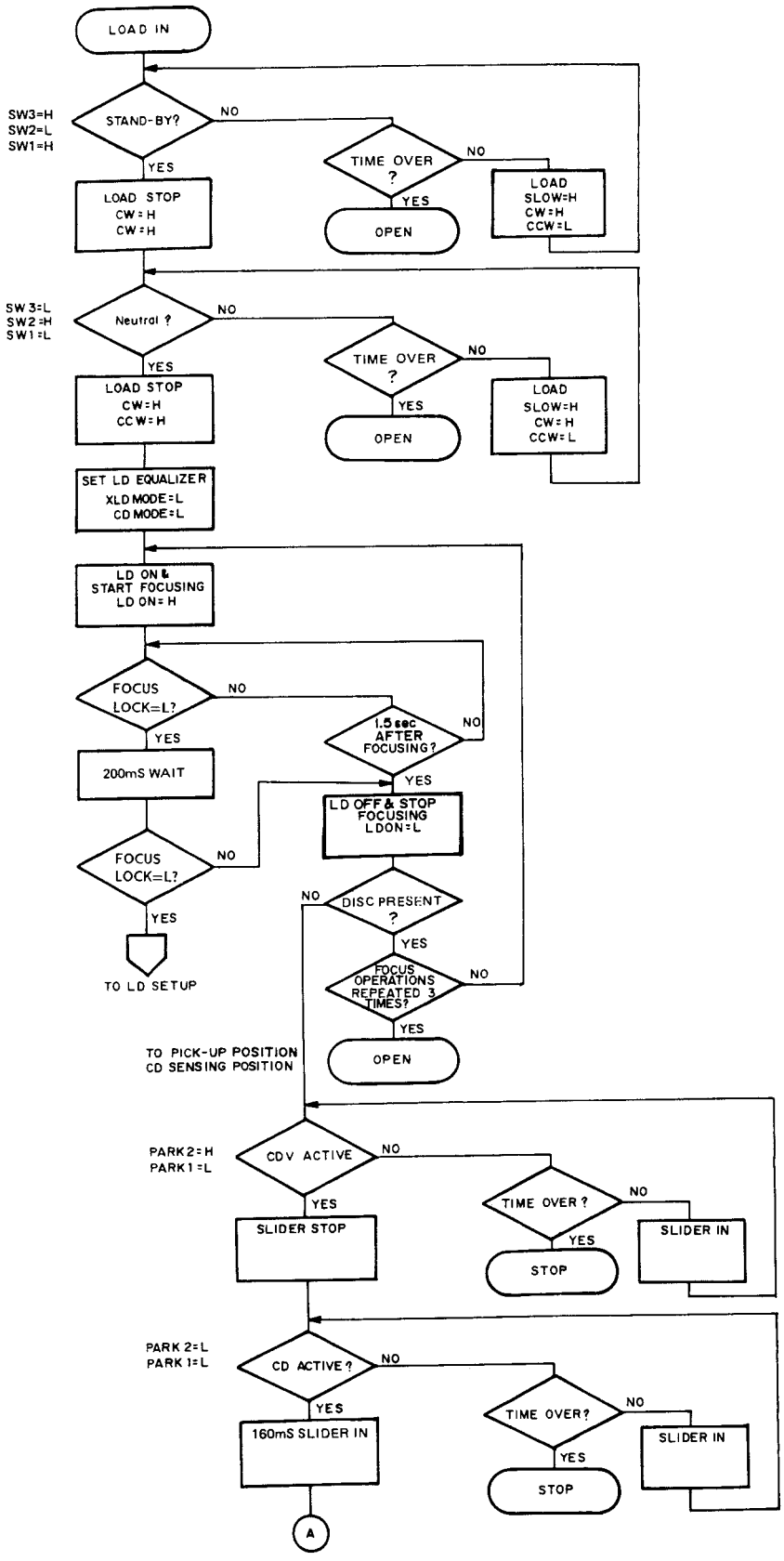
*5

CDMODE	XLDMODE	Disc Mode
L	L	LD
L	H	CDV Video part
H	L	Not defined
H	H	CD/CDV Audio part

*6



• Flowchart from tray open status to tray in operation



- From open status till tray-in operation is completed

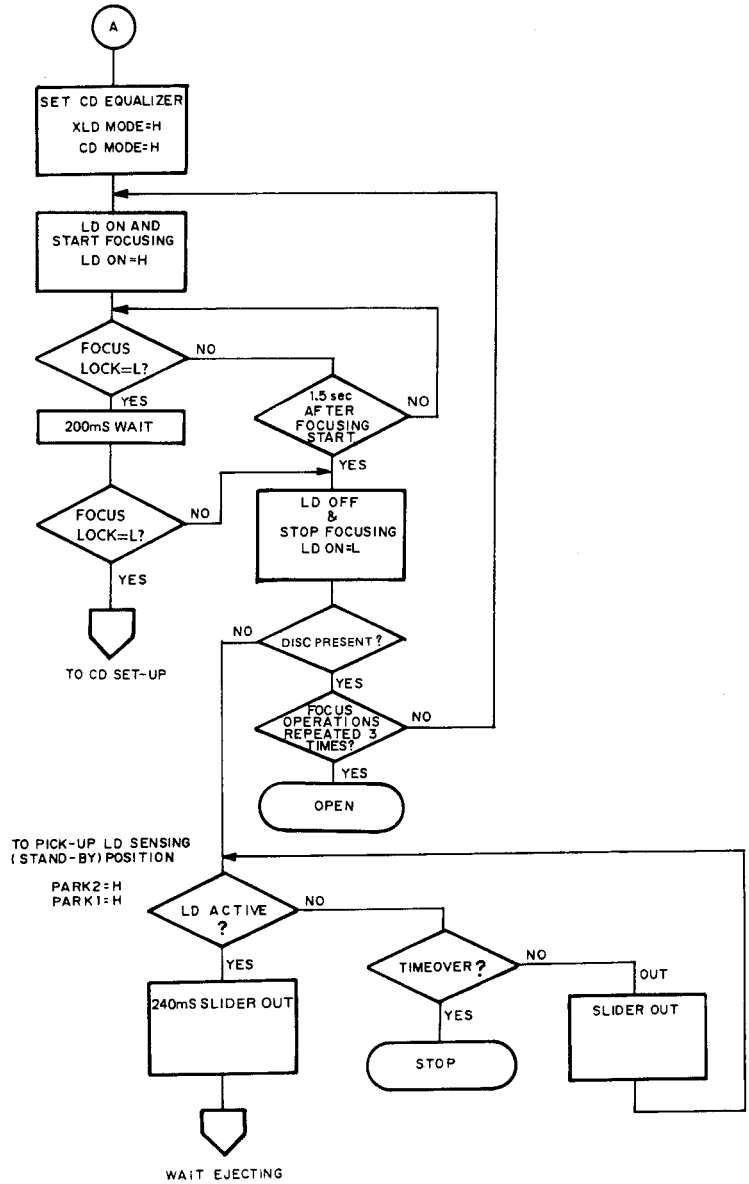
- If the loading operation is not finished within 10 seconds, it is regarded as abnormal and the tray is opened again

- Clamping

- Pick-up position during LD focus operation: around R65
  R: The distance from center of the spindle motor.

- **During focus sweep operation, when FOCUS LOCK goes "L", it is regarded that a disc is present.**
- With a disc present, if the focus lock is not obtained after sweeping the focus three times, it is regarded as abnormal and opens the tray.
- Slider operation limit timer: about 10 seconds

- If the slider operation is not finished within a fixed time, the player enters the stop mode and no key inputs other than OPEN key are accepted.

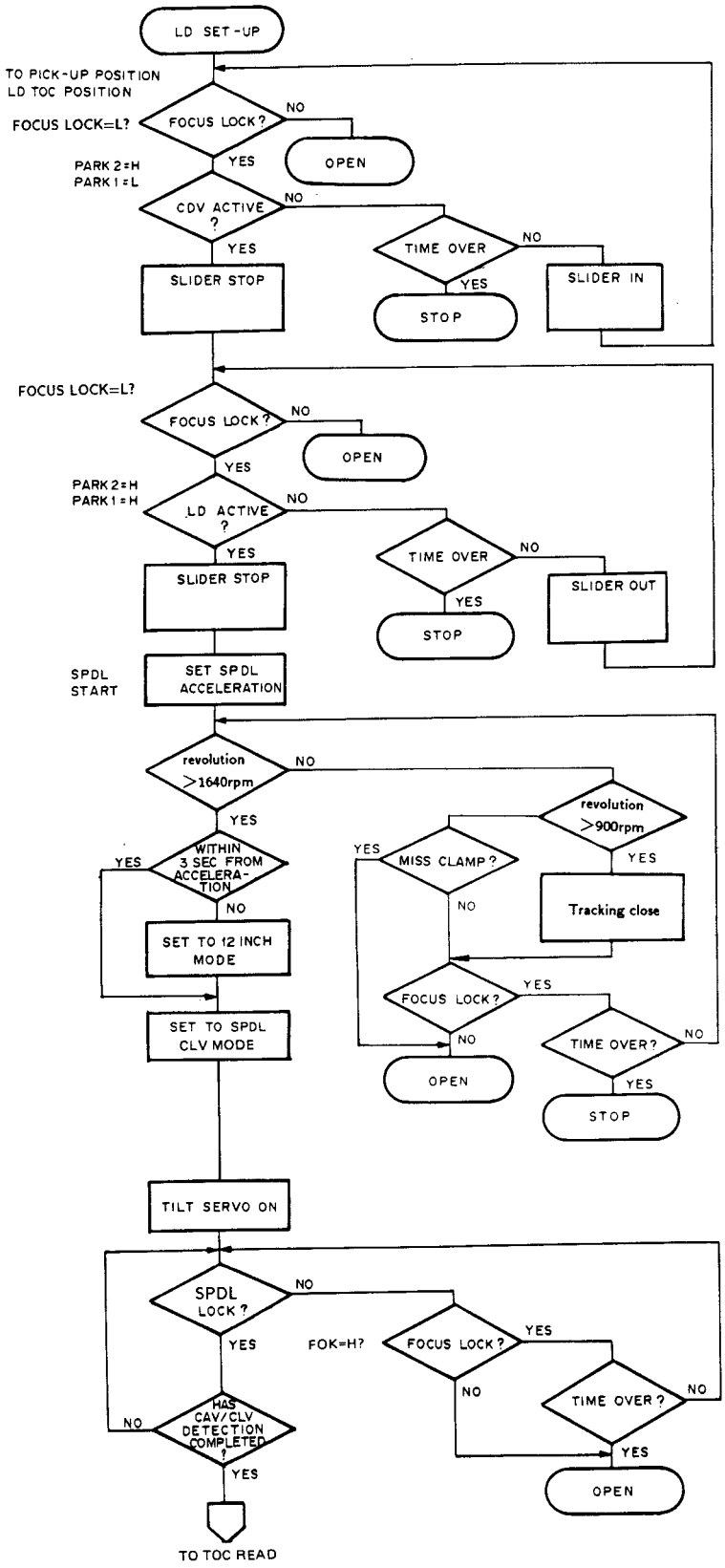


- Pick-up position during CD focus operation: around R30
- CD focus operation is performed in the same way as that for LDs.
  R: The distance from center of the spindle motor.

- LD sense position: around R65
  R: The distance from center of the spindle motor.

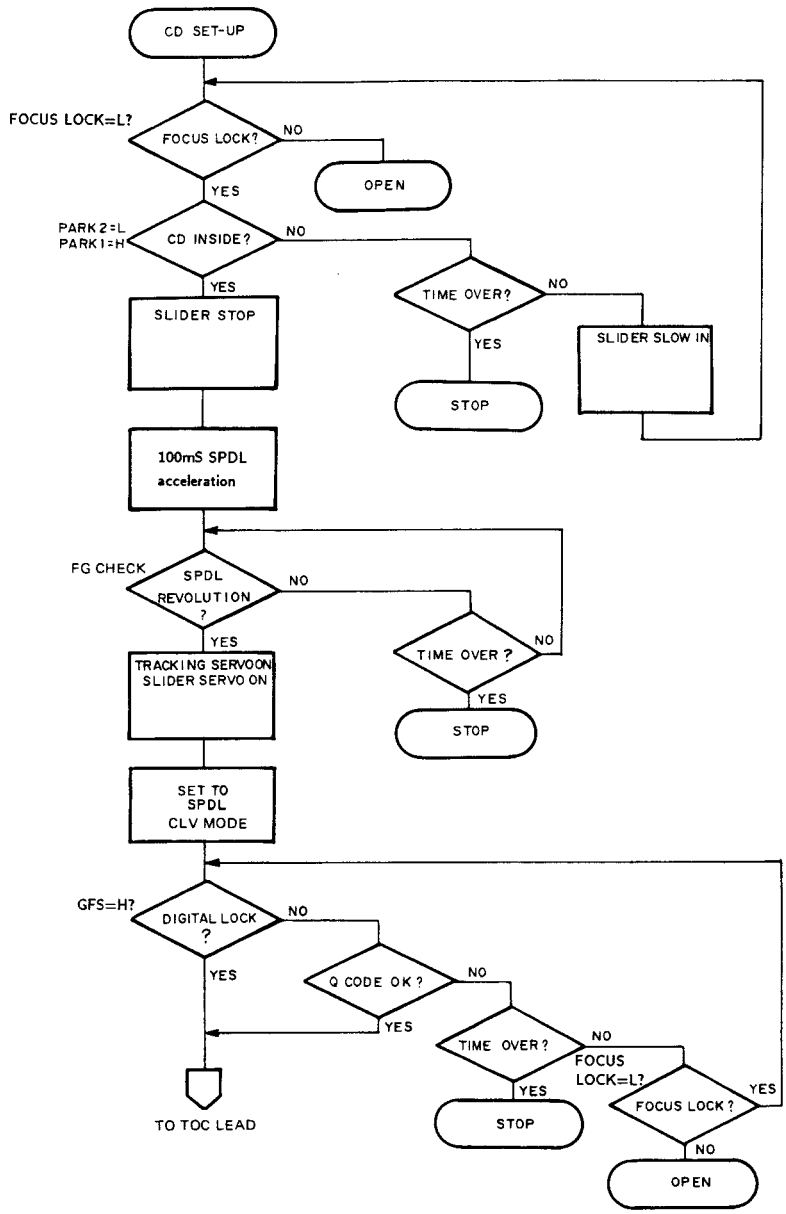
- Timer: about 10 seconds.
  Timer → The TIME OVER time mentioned on the left.

• Flowchart of LD Setup



- When the focus is unlocked while the pick-up is moving to the spindle motor start position, it is judged that LD and CD discs have been loadded simultaneously and the tray is opened.
- Timer : about 10 seconds
  Timer → The TIME OVER time mentioned on the left.
- Timer : about 10 seconds
- Until the disc rotation speed exceeds 900 rpm, the tracking servo is set to the open mode and spindle motor is forced acceleration.
- When the pick-up moves across more than 1600 rpm tracks in one revolution of the disc, it is judged as mis-clamping and the tray is opened.
- If the focus is unlocked during setup operation, it is judged that there is a scratch on the disc or that the unrecorded surface of the single-side disc is being played, and the tray is opened.
- When the disc rotation speed does not exceed 1640 rpm within 60 seconds after the spindle motor starts accelerating, the player enters the stop mode.

• Flowchart of CD Setup

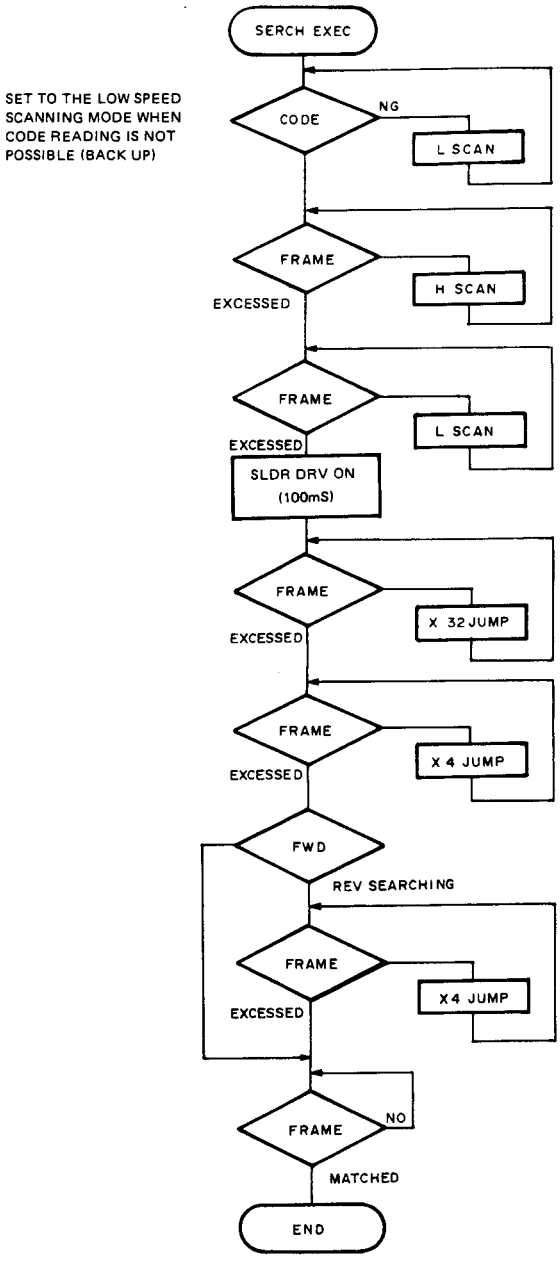


- When the pick-up is fed to the inside of the disc (CD), the disc speed is lowered by driving the slider motor in PWM drive.
- **When a CD is loaded, the spindle motor is accelerated for 100 mS forcibly.**

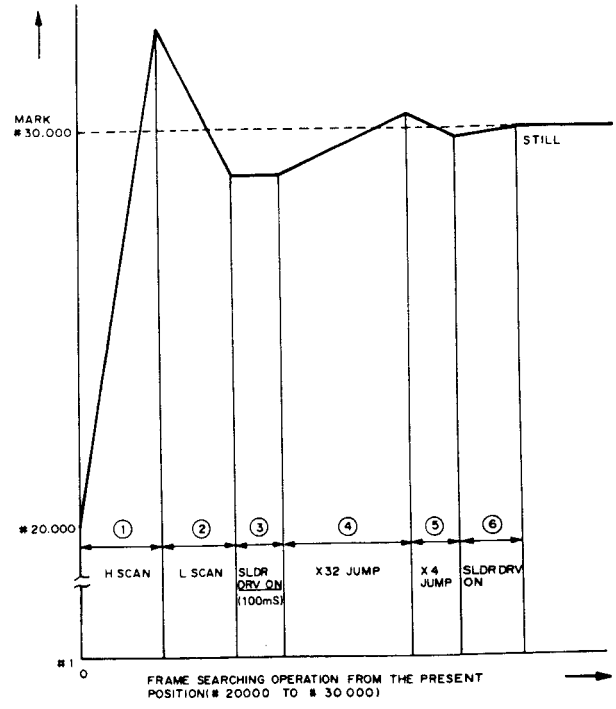
- When the FG input signal is not inverted 6 times within 2 seconds, the player enters the stop mode.

- When the digital lock or Q-code OK signal is not detected within 2 seconds after the tracking/slider servo is closed, the player enters the stop mode.
- If the focus is unlocked during disc rotation, it is judged that the unrecorded surface of the disc has been placed on the tray, and the tray is opened.

• Flowchart of Frame Search Operation



- Slider motor drive duty : 1/8
- Slider motor drive duty : 100%
- Slider motor drive duty : 1/8
- Waiting for 100 mS (tracking/ slider servo ON)
- 32-track jump
- 4-track jump
- 4-track jump (Reverse search only)



FRAME SEARCH OPERATION